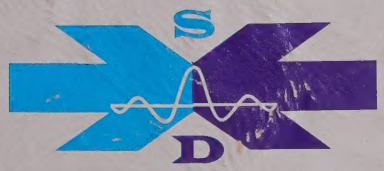
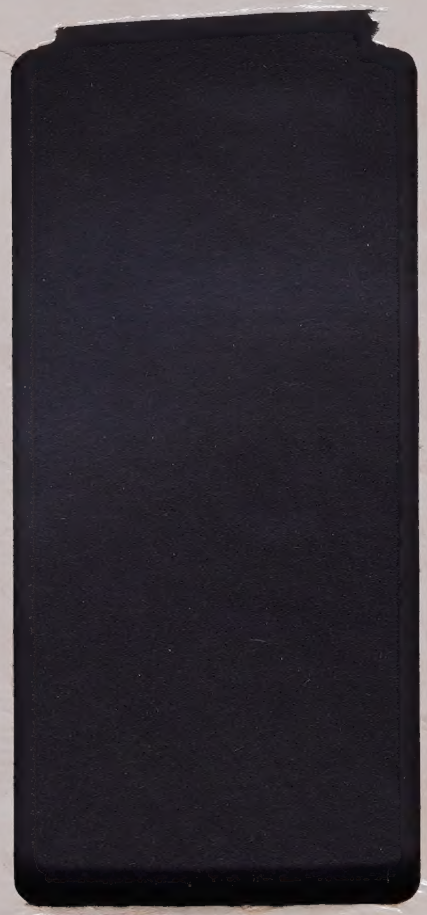
INSTRUCTION MANUAL

SD102

DYNAMIC ANALYZER TUNER



SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO



SERIAL NUMBER 85

Schematic Change Letter "E"

INSTRUCTION MANUAL

SD102

DYNAMIC ANALYZER TUNER

PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

8159 Engineer Road, P. O. Box 671
San Diego, California 92112
Area Code 714, 278-2501

1 November 1964

Model SD102 Dynamic Analyzer Tuner
(Shown with SD102-10 General Purpose TFM Plug-In)

PACKING

The Model SD102 Dynamic Analyzer Tuner (DAT) is shipped fully assembled in a polystyrene carton which protects the instrument against all normal shipping hazards. To determine possible damage during shipment of the instrument, the procedures given below should be followed:

a. Place the carton upright on the floor and inspect the exterior, making note of any visible damage.

b. Remove and retain all forms and invoices attached to the carton by the carrier.

c. Unseal the top portion of the carton and remove.

d. Lift the instrument out of the carton and place it on a work bench or other flat surface.

e. Inspect the exterior of the Dynamic Analyzer Tuner (DAT) carefully, noting all visible damage.

f. The Dynamic Analyzer Tuner (DAT) may now be checked for functional operation by following the procedure outlined in Section II.

CLAIM FOR DAMAGE IN SHIPMENT

The instrument should be tested as soon as it is received. If it fails to operate properly, or is damaged in any way, a claim should be filed with the carrier. A full report of the damage should be obtained by the claim agent, and this report forwarded to Spectral Dynamics Corporation of San Diego. The buyer will be advised of the disposition to be made of the equipment and arrangements shall be made for repair or replacement. Include Name, Model Number and Serial Number when referring to this instrument for any reason.

WARRANTY

Spectral Dynamics Corporation of San Diego warrants each instrument manufactured by them to be free from defects in material and workmanship for one year after delivery to the original purchaser. Our liability under this warranty is limited to servicing and adjusting the instrument returned to the factory with transportation charges prepaid by the purchaser. This warranty specifically excludes any liability in regard to electron tubes, batteries, fuses and lamps. If the fault or a portion thereof is determined by us to have been caused by misuse or abnormal conditions of operation, an estimate will be submitted to the purchaser prior to starting the work on the repairs.

If any fault develops, the following steps should be taken:

1. Notify us or our representative in your area, giving full details of the problem, including name, model and serial number of the equipment. Upon receipt of this information, we will submit service data or shipping instructions.

2. On receipt of shipping instructions, forward the instrument prepaid, to the factory or authorized repair station indicated on the instructions.

SHIPPING

All shipments to the factory should be made via Air Freight. The instrument should be replaced in its original shipping carton or in a strong exterior container surrounded by two or three inches of excelsior or similar shock-absorbing material.

TABLE OF CONTENTS

Section			Page
I	DESCRIPTION & CHARACTERISTICS		1
	1.1	General	1
	1.2	Purpose	1
	1.3	Specifications	2
II	OPERATION		3
	2.1	Installation	3
	2.2	General Operating Procedures	4
	2.3	Frequency/Ratio Counter - General Information	4
	2.4	Frequency/Ratio Counter Operating Procedures	6
	2.4.1	Frequency Measurement	6
	2.4.2	Frequency Ratio Measurement	7
	2.4.3	Period Measurement	8
	2.4.4	Self Testing Feature	10
III	THEORY OF OPERATION		11
IV	MAINTENANCE		17
	4.1	Trouble Shooting - General	17
	4.2	Basic Trouble Shooting Procedure	17
	4.2.1	Initial Checks That Equipment Is Properly Set Up	17
	4.2.2	Functional Operational Checks	17
	4.3	Detailed Trouble Shooting Procedure	18
	4.3.1	Localizing The Trouble Area	19
	4.4	Calibration	20
	4.5	Adjustment of Power Supply Voltages	20
	4.6	Adjustment of The Sine Shaper Network	21
	4.7	Cleaning	22
V	REPLACEABLE PARTS		23
	5.1	General	23

LIST OF TABLES

Number	Title	Page
2.1	DAT Operational Connections	3
5.1	Replaceable Parts	23

LIST OF ILLUSTRATIONS

Figure	Title	Page
1	Front and Rear View of Model SD102 Analyzer Tuner	5
2	Input Waveform Symmetry Requirement for TFM Sine Wave Plug-ins	14
3	Input Waveform Symmetry Requirement for TFM Pulse Plug-ins	14
4	Top View	25
5	Partial Top View	26
6	Bottom View	27
7	Component Locations on Circuit Card Assembly No. 22042-1 (A8)	28
8	Component Locations on Circuit Card Assembly No. 22041-1 (A9)	29
9	Component Locations on Circuit Card Assembly No. 22040-1 (A10)	30
10	Component Locations on Circuit Card Assembly No. 22039-1 (A13)	31
11	Interconnecting Diagram	33
12	Block Diagram	34
13	Dynamic Analyzer Tuner - TFM Mode Detailed Block Diagram	35
14	Linear/Log Sweep Generator Detailed Block Diagram	36

LIST OF ILLUSTRATIONS (CONTINUED)

Figure	Title	Page
15	Power Supply Schematic Diagram	37
16	Circuit Card No. 22042-1 (A8) Schematic Diagram	38
17	Circuit Card No. 22041-1 (A9) Schematic Diagram	39
18	Circuit Card No. 22040-1 (A10) Schematic Diagram	40
19	Circuit Card No. 22039-1 (A13) Schematic Diagram	41

SECTION I

DESCRIPTION & CHARACTERISTICS

1.1 GENERAL

The Model SD102 Dynamic Analyzer Tuner (DAT) combines with a series of functional plug-in modules to form a wide range frequency multiplying device, with additional capabilities as a sweeping-type oscillator with linear and logarithmic sweep modes.

The basic DAT chassis houses a frequency/ratio counter module, power supply module, plug-in type operational amplifiers, and associated circuits located on plug-in printed circuit cards. Solid state circuitry is used throughout.

The SD102 DAT becomes a complete instrument with the addition of a front panel plug-in unit, selected by the customer to meet specific frequency multiplication or signal generation requirements.

Tracking Frequency Multiplier (TFM) type plug-ins enable the DAT to produce an output frequency that is (M) times the input frequency to the unit. This multiplication factor (M) is variable over a specific range and is indicated on the 5-digit frequency/ratio counter. As the input frequency varies, the output frequency also varies, maintaining the selected multiplication ratio (M). A dc analog proportional to the input frequency is provided for driving X-Y plotters and recorders.

When combined with the Linear/Log Sweep Generator (L/LSG) plug-in, the DAT becomes an electronically swept oscillator. The sweep rate is adjustable over a wide range and can be programmed for either linear or logarithmic sweep rates by a front panel control. Sine, square and triangle wave outputs are available simultaneously as well as dc proportional to the output frequency.

1.2 PURPOSE

The SD102 DAT and the series of TFM plug-ins are designed to provide a tuning signal for Spectral Dynamics Corporation Analyzers/Tracking Filters when the available tuning signal frequency is a multiple or sub-multiple of the desired tuning frequency.

Input signal must be repetitive in nature and may come from tachometer generators, ignition systems, proximity pickups, accelerometers, etc., providing that their waveform, polarity and voltage conform to the requirements of the particular plug-in type.

The L/LSG type plug-in adapts the DAT to tasks requiring a sweep oscillator with an output frequency range of 1 to 30,000 cps. With both linear and logarithmic sweep rates available, the DAT with L/LSG plug-in is used to tune Spectral Dynamics' Analyzers/Tracking Filters for power, spectral density analysis, harmonic analysis, mechanical impedance measurements, etc.

1.3 SPECIFICATIONS

Performance specifications of the SD102 DAT are determined by the type of plug-in being used. Separate instruction manuals are provided for each type of plug-in unit and contain complete specifications and operating instructions for the DAT when using a particular plug-in.

General specifications for the DAT are as follows:

Power requirements:	115 volts, 50/60 cps, 165 watts, approx.
Connectors:	Type BNC, located on rear of chassis
Dimensions:	7" high, 19" wide, 14" deep
Shipping weight:	25 pounds, including plug-in unit

The following specifications apply to the frequency/ratio counter:

Frequency gate time:	0.1, 1.0 and 10 seconds
External input sensitivity:	Sine wave: 0.1 v rms, 3 cps to 100 kc Square wave: 0.1 v p-p, 0 to 100 kc
Ratio (A/B or B/A) and Period (A only):	1, 10 and 100 periods
Type of display:	5 decade Nixie
Display time:	0.2 to 6 seconds, and infinite
Time base:	100 kc crystal controlled oscillator Aging: ± 2 ppm/week Temp: ± 20 ppm, 15° to 40° C
Measurement accuracy:	Frequency: ± 1 count ± time base accuracy Ratio: ± 1 count

SECTION II

OPERATION

2.1 INSTALLATION

The SD102 DAT may be mounted in a standard 19 inch relay rack or used as a bench type instrument. Provide adequate equipment ventilation. Do not cover top ventilation holes or obstruct airflow from fan on rear panel.

To facilitate calibration and maintenance it is recommended that the DAT be mounted on slides when installed in the rack configuration. Slide mounting holes have been provided on the DAT chassis. Slides should be modified if necessary to fit these holes rather than drilling new holes in the DAT chassis.

Operational connections are as shown in Table 2.1 and Figure 1. An interconnecting diagram is shown in Figure 11.

Table 2.1. DAT Operational Connections

CONNECTION	FUNCTION
J12	Input signal (Signal A) used with TFM plug-ins
J13	External A input for frequency/ratio counter. Used as a convenience feature for frequency or period measurements of external signals.
J14	Sine wave B output
J15	Square wave B output
J16	Triangle wave B output
J17	+DC proportional to frequency
J18	Conditioned signal A output (TFM plug-ins only)
J19	Variable amplitude sine wave output (used only with L/LSG plug-in Model SD102-20)
J20	Not used

Table 2.1. DAT Operational Connections (Continued)

CONNECTION	FUNCTION
J21	Not used
J22	Line power input 105-125 volts, 50/60 cps, 165 watts.

2.2 GENERAL OPERATING PROCEDURES

a. Install frequency/ratio counter in left-hand DAT opening. Tighten locking device on counter front panel.

b. Install TFM or L/LSG plug-in in right-hand opening. Tighten locking device.

c. Turn Power switch to RESET. After a pause of several seconds, turn to the ON position. The Nixie tubes in the counter will now glow. NOTE: Power is only applied to the counter module when the power switch is in the ON position.

d. Test the counter as follows: Place the Frequency-Period switch in the PERIOD/TEST position. Set the function switch to FREQ B with a time base of 1 second. Adjust the DISPLAY TIME control for a short display. The Nixie readout should read 10000. With a 10 second time base the reading should be 00000; a 0.1 second time base will show 01000.

e. Circuit ground and chassis ground are made common by a shorting bar located on the rear of the DAT. Reposition this bar if it is desired to float the DAT circuit.

f. The DAT is now ready to operate. Section 2.4 gives complete operating instructions for the frequency/ratio counter. Refer to the instruction manual covering the selected TFM or L/LSG plug-in for details of plug-in operation.

2.3 FREQUENCY/RATIO COUNTER - GENERAL INFORMATION

The frequency/ratio counter is basically a 100 kc 5-digit frequency counter. It contains additional circuitry and control features that enable it to measure the ratio between two signals, the period of a signal, and to self test its own operation. All connections to the DAT and to line power are made automatically by a rear connector when the counter is properly installed in the DAT chassis. Removal of the counter module will not affect the performance of the remaining DAT circuitry.

Used with a TFM plug-in, the counter will measure the:

Frequency of signal A (TFM input signal)

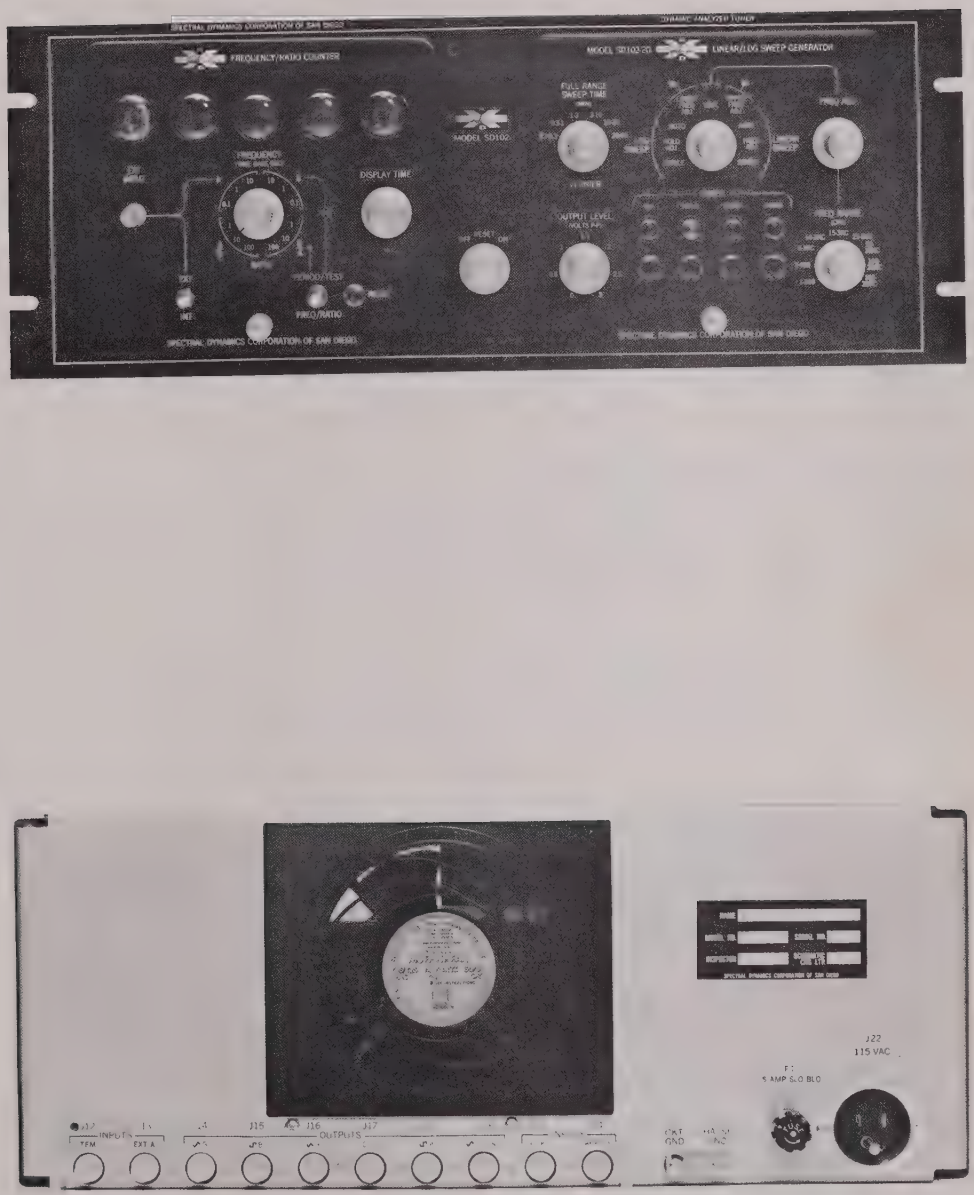


Figure 1. Front and Rear View of Model SD102 Analyzer Tuner

Period of signal A

Frequency of signal B (DAT output signal)

Ratio between signal A and signal B

Used with the L/LSG plug-in, the counter will measure the:

Frequency of signal B (DAT output signal)

Period of signal B

Set for "External A" operation, the counter will measure the:

Frequency of the external A signal

Period of the external A signal

Ratio between the external A signal and the DAT output signal, signal B, being produced by any type of plug-in.

Complete maintenance and calibration instructions and theory of operation for the counter will be found in following sections of this manual.

2.4 FREQUENCY/RATIO COUNTER OPERATING PROCEDURES

The counter is normally used to monitor the ratio or frequency of signals being processed or generated by the DAT. Examples given in the following operating procedures assume the use of a TFM-type plug-in, with an input signal (signal A) of 20 cps and a DAT output signal (signal B) of 4000 cps.

See Section II of the counter instruction manual for a complete description of counter front panel controls.

2.4.1 Frequency Measurement

To measure the frequency of a signal, the counter counts the number of cycles of the signal that occur during a precisely controlled time interval. Time intervals of 0.1, 1.0 and 10.0 seconds can be selected by the front panel Function Selector switch. For example, the counter would read 00020 if set to measure the frequency of a 20 cps signal and allowed a counting time (time base) of 1 second. If allowed to count for a 10 second period, the counter would read 00200, having counted 200 cycles of the 20 cps signal in 10 seconds. A time base of 0.1 second would produce a reading of 00002, the counter having counted only 2 cycles of the 20 cps signal during the 0.1 second of counting time allowed.

To measure the frequency of signal A, proceed as follows:

a. Set Function Selector switch to FREQUENCY A, with a time base of 1 second.

b. EXT - INT switch to INT

c. PERIOD/TEST - FREQ/RATIO switch to FREQ/RATIO

d. Adjust DISPLAY TIME control to give adequate display time. The display time can be varied from 0.2 seconds to 6 seconds. When only one reading is desired the control is turned fully CCW to the detent position, placing the counter in the "hold" mode. The counter will repeat the measurement only when the RESET button is pressed.

e. The frequency of signal A is now displayed directly in cycles per second. The two alternate time base positions may be used as required.

Measure the frequency of an external A signal by setting the counter controls as above, except that the EXT - INT switch is placed in the EXT position. The external A signal may be applied to the counter via the front panel BNC connector on the counter or via J 13 on the rear of the DAT chassis.

The frequency of signal B is measured as in steps a. thru e. above, with the Function Selector set to an appropriate time base under FREQUENCY B.

2.4.2 Frequency Ratio Measurement

The frequency ratio of one signal to another can be determined by measuring the frequency of each one and dividing the lower frequency into the higher one. The answer gives the number of cycles of the higher frequency signal that occur during one cycle of the lower frequency signal.

Example: Signal A 20 cps

Signal B 4000 cps

Dividing B by A gives an answer of 200. This means that during one cycle of signal A, 200 cycles of signal B will occur. The ratio of B to A is, therefore, 200 to 1.

The frequency/ratio counter can be programmed to display this ratio directly and continuously, eliminating the separate frequency measurements and mathematics described above. It does this by having the lower frequency signal control the gate to the counter input, and counting the higher frequency signal.

In the example above, signal A would control the gate. With signal A holding the gate open for one cycle (one period) the counter would receive and count 200 cycles of signal B. This number is displayed on the counter as 00200 and is read directly as the ratio of B to A.

For greater accuracy or for averaging purposes, the counter can be programmed to hold the counter gate open for 10 or 100 periods of the controlling signal. In the example above, the counter would read 02000 and 20000 respectively. The ratio of B to A is still 200 to 1, the operator mentally placing the decimal point one or two places to the left as required.

TFM plug-ins are capable of multiplying input signals by factors of less than 1.0, making signal B lower in frequency than signal A. In this case signal B controls the gate and the resulting number displayed by the counter is the ratio of A to B.

Signal B (the DAT output frequency) is internally connected to the counter. Signal A, the input frequency to a TFM plug-in, is also connected internally to the counter when the EXT - INT switch is in the INT position. By placing this switch in the EXT position the operator can determine the ratio between signal B and an external signal A.

To measure the ratio between signals A and B, proceed as follows:

a. Set the Function Selector switch to RATIO A/B or B/A with a "period time base" of 1.

b. EXT-INT switch to source of signal A

c. PERIOD/TEST - FREQ/RATIO switch to FREQ/RATIO

d. Set DISPLAY TIME control for short display time

e. Observe reading displayed on the counter. If counter reads 00000 reverse position selected in step a. Number displayed by counter will be the ratio between the signals as selected by the Function Selector switch. (In the example mentioned previously, the counter will read 00200 with the Function Selector switch in the B/A position, indicating the ratio of B to A is 200 to 1.)

f. Use alternate 10 and 100 period time base positions if greater accuracy is required.

2.4.3 Period Measurement

The period of a signal is the reciprocal of its frequency. It is the amount of time it takes for one cycle of the signal to occur.

Example: Signal A is 20 cps

The reciprocal of A is 1/20 which is 0.05

Therefore the period of A is 0.05 seconds, or 50 milliseconds.

When measuring the frequency of signals below 316 cps, greater accuracy can be obtained by measuring the period of the signal and converting it to frequency. The lower the frequency the more this is true.

Period is measured by using the unknown signal to control the counter gate. The counter counts 10 kc clock pulses while the gate is open for one period of the unknown signal. Multiplying the counter reading by the period of the clock pulse (100 microseconds) gives the period of the unknown signal.

Example: Counter reading is 00500

500 x 100 usec = 50,000 usec, or 50 msec

50 msec = the period of a 20 cps signal

The counter may be "read" directly in milliseconds by mentally placing a decimal point between the fourth and fifth digits, i.e. 0050.0.

To measure the period of signal A, proceed as follows:

a. PERIOD/TEST - FREQ/RATIO switch to PERIOD/TEST

b. Set the Function Selector switch to RATIO B/A, 1 period.

c. EXT-INT switch to source of signal A

d. Set DISPLAY TIME control for short display time.

e. Counter will now indicate the number of clock pulses occurring during one cycle of signal A. Dividing the counter reading by 10 gives period of signal A directly in milliseconds.

For greater accuracy or resolution the gate may be held open for 10 or 100 periods of signal A. Direct reading in milliseconds is accomplished by moving the decimal point two and three places to the left respectively (dividing the counter reading by 100 and 1000).

Period measurements may only be performed on signal A inputs.

The output of the L/LSG type plug-in is internally connected to both the A and B inputs of the counter and may, therefore, be measured as signal A.

To measure the period of signal B when using a TFM plug-in, connect the signal to the EXT A counter input and measure as above.

2.4.4 Self Testing Feature

In the self-test mode the counter reads the frequency of internally generated 10 kc clock pulses. Correct readings indicate that most of the counter circuits are working normally. However, this is not a test of the reference oscillator accuracy. See the counter manual for 100 kc oscillator calibration instructions.

a. Set the Function Selector switch to FREQUENCY B, 1 second time base.

b. PERIOD/TEST - FREQ/RATIO switch to PERIOD/TEST

c. Set DISPLAY TIME control for short display.

d. Counter should read 10000. A time base of 10 seconds should produce a reading of 00000. A 0.1 second time base would read out 01000.

SECTION III

THEORY OF OPERATION

The SD102 Dynamic Analyzer Tuner (DAT) is a basic chassis assembly containing a frequency/ratio counter, power supply, plug-in type operational amplifiers, and associated circuits located on plug-in printed circuit cards. Space is provided for an additional plug-in module which determines the exact function and specifications of the complete instrument. See Figure 12 for block diagram.

The choice of plug-in module determines whether the SD102 will be a frequency multiplying device (TFM Plug-In) or a sweep oscillator (L/LSG Plug-In). The theory of operation presented in the following paragraphs assumes the use of a frequency multiplier plug-in module with an input (sine wave) frequency range of 10 to 100 cps and a multiplying range of 0.1 to 100.

Assume that the input frequency (signal "A") is 20 cps and it is desired to multiply it by 10 to a new frequency (signal "B") of 200 cps.

The input signal (50 mv to 65 volts rms) is heavily clipped, amplified and squared-up by the two stage input amplifier. An emitter follower couples the resulting square wave signal to a Schmitt trigger where it is further amplified with fast rise and fall times. The frequency at this point is still that of signal A.

The Schmitt trigger output is differentiated to produce a negative pulse for each negative-going axis crossing. In addition, the output is inverted and differentiated again, producing a negative pulse for each positive-going axis crossing. Both pulses are combined across a common resistor, giving a negative pulse for each axis crossing of signal A. (Pulse freq = A times 2)

The pulse train is amplified, inverted and used to control the triggering (firing) of a monostable multivibrator. Each time the monostable is triggered it produces a pulse of constant duration, or width. The higher the triggering frequency, the higher the monostable duty cycle; therefore, the more pulse energy that is produced per unit time (pulses per second).

The monostable output pulses are passed to an emitter follower and then to a low pass filter. The negative half of each pulse is tightly clamped to ground. The low pass filter receives a steady train of positive going pulses, each of constant width and occurring at each axis crossing of signal A. If the frequency of signal A increases, the

filter receives more of the constant-width pulses per second, and conversely if the frequency decreases. Each pulse applied to the low-pass filter produces a dc voltage at the output of the filter. The more pulses per second in, the higher the dc output from the filter.

The input signal has now been converted to a dc voltage. This voltage depends on the frequency of the input signal, not its amplitude. The dc voltage from the filter will vary linearly with any change in the input frequency.

The filter output dc voltage, representing the frequency of signal A, is amplified by an operational amplifier and connected to one terminal of a solid-state single pole double throw switch, hereafter referred to as the Frequency Controlled Switch, or FCS. The same dc voltage is inverted at unity gain by a second operational amplifier and applied to the opposite pole of the FCS. These opposite-polarity equal-amplitude dc voltages will now be converted into a triangular wave, the frequency of which is 200 cps, and which will track any changes in the input frequency (signal A) while maintaining a multiplication factor of 10. This will be the dc to frequency portion of the SD102 circuit.

The frequency controlled switch is in reality a pair of transistors, a PNP and a NPN, with emitters tied together to form the "pole" of the SPDT switch. The PNP collector is tied to the -dc voltage proportional to frequency, the NPN collector to the +dc voltage proportional to frequency. Both bases are connected together and are driven from one side of a bistable multivibrator. Assume that the bistable is resting in a state that drives the "switch" bases positive, turning the NPN on and the PNP off. The +dc voltage proportional to frequency now appears at the pole of the switch.

From the pole of the switch the +dc voltage is applied to an operational integrator. With + dc applied to its input, the integrator generates a negative-going ramp. This is the negative-going portion of what becomes a triangle wave at the desired output frequency (signal B). Upon reaching a predetermined negative voltage, the ramp causes control circuits (described below) to switch the FCS to its opposite position, thereby reversing the polarity of the integrator input voltage. The integrator now integrates in the opposite direction producing a positive-going ramp until it, in turn, is reversed by the sensing and control circuits.

Two Schmitt triggers monitor the output voltage of the integrator, one set to trip at a predetermined positive voltage, the other at a negative voltage. They, in turn, trigger the bistable multivibrator connected so as to control the position of the FCS. The bistable assumes a new state whenever either Schmitt trigger fires. Therefore the output of the integrator is constantly being monitored by circuitry that will reverse the polarity of the integrator input voltage whenever the output voltage reaches preset plus or minus limits.

The frequency of signal B is determined by how fast the integrator output voltage reaches the preset limits, triggering the reversal process. Stated another way, the

slope (volts per unit time) of the integrator output ramp determines the frequency of signal B. Two major factors determine this slope: (1) The amplitude of the dc voltage proportional to frequency applied to the integrator, and (2) The integrator RC time constants.

Item 1. depends on the frequency of signal A. In our example this is a steady 20 cps. Obviously, if signal A varies in frequency, the dc proportional to this frequency will vary and in turn will change the slope of the integrator output ramp, thus changing the frequency of signal B.

The integrator RC time constants (Item 2.) are controlled by the settings of the Ratio Range and Ratio Vernier controls on the plug-in unit. Therefore with a given signal A, these controls can be adjusted to make signal B any frequency within the stated ratio or frequency limits of the plug-in. In this example the controls are adjusted to make signal B 200 cps, equal to signal A times 10, or a ratio of 10 to 1 between signal B and A. This ratio between B and A will remain the same as long as the frequency of these signals remains within the stated limits for the particular plug-in.

The output signal of the integrator, being made up of equal, linear positive and negative ramps, is a triangle wave. The amplitude of this waveform is constant, depending only on the trigger points of the voltage-sensing Schmitt triggers. This triangle wave is available at a rear connector.

To produce a sine wave output at the frequency of signal B, the triangle wave is also applied to a sine shaper circuit. This circuit changes the triangle wave into a sine wave having less than 1% total harmonic distortion. Three sets of reverse biased diodes "break over" the triangle wave at preset points on both the negative and positive slopes. The break points are "softened", or rounded, by momentarily applying negative feedback to the sine-wave output cathode follower as the breaks occur.

Signals A and B are internally connected to the 5-digit frequency/ratio counter module. Front panel controls allow the operator to read the frequency of signal A or B or the multiplication ratio between the two signals.

BNC-type coaxial connectors on the rear panel of the SD102 provide access to all signal inputs and outputs. Output impedances are all 1 K ohm or less except the dc proportional to frequency, which is 10 K ohms.

As stated at the beginning of this section, the theory of operation presented above assumes the use of a standard sine-wave input TFM plug-in. Generally speaking, "sine wave" TFM plug-ins will accept any repetitive waveform with ± 5% symmetry. This includes sine, square and triangular waveforms. Figure 2. defines the symmetry requirements.

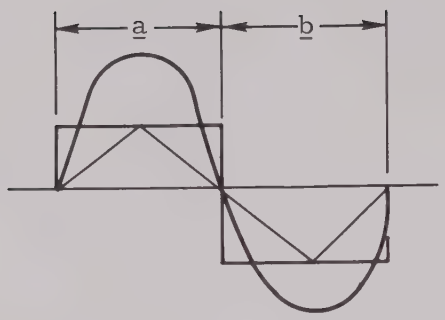


Figure 2. Input Waveform Symmetry Requirement for TFM Sine Wave Plug-ins.

For TFM's with sine-input capability the input must be symmetrical in its axis crossing within ± 5%. Figure 2. illustrates this signal requirement: a and b must be within ± 5% in value.

TFM plug-ins designed to work from pulse signals have slightly different input requirements and one major difference in the handling of signal A.

TFM pulse plug-ins require positive going pulses with a duty cycle of 10 to 60%. Figure 3. defines the duty cycle requirements. Note -- "pulse" TFM's will also accept sine, square or triangular waveforms.

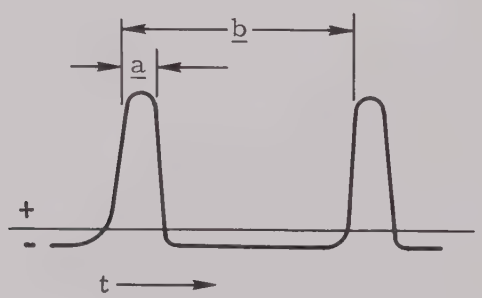


Figure 3. Input Waveform Symmetry Requirement for TFM Pulse Plug-ins.

For TFM's with pulse-input capability the pulse width a must be between 10% minimum and 60% maximum of the repetition width b per Figure 3. The pulse must also be positive

Pulse-type TFM plug-ins contain a pulse-to-squarewave conversion circuit. The input signal (pulse, sine, square, etc.) is heavily clipped, amplified, squared-up, differentiated once, and used to trigger a bistable multivibrator. The bistable is triggered only once per complete cycle of signal A, and therefore it is running at a frequency of A/2. The bistable output passes to the SD102 input amplifier and is handled just as described in the preceding theory of operation.

To repeat, pulse-input plug-ins divide the input frequency by 2 in the process of converting it to a square wave. The frequency to dc portion of the SD102 therefore runs at "A" divided by 2. This, in turn, defines the characteristics of the low pass filter used to convert the monostable multivibrator constant-width pulses to dc. The lower

the frequency for which the low pass filter is designed, the "slower" the filter is to respond to changes in frequency. This characteristic determines the maximum speed (cps/s) that the SD102 will track a changing input frequency.

One other type of plug-in should be mentioned in this discussion. The Model SD102-20 is a linear/log sweep generator plug-in that uses only the dc to frequency portion of the SD102 It generates and controls its own linear or logarithmic ramp function, then passes it on to the SD102 dc-to-frequency conversion circuit where the output frequency is developed. Full details on this and all other plug-ins will be found in their respective instruction manuals.

SECTION IV

MAINTENANCE

4.1 TROUBLE SHOOTING - GENERAL

A systematic approach should be followed when trouble shooting the SD102 DAT. Most problems are caused by a lack of understanding of the unit on the part of the operator or the maintenance technician. Before attempting any repair or adjustment of the DAT, the technician should become thoroughly familiar with the theory of operation and basic specifications for the unit, and for the functional plug-in being used.

4.2 BASIC TROUBLE SHOOTING PROCEDURE

4.2.1 Initial Checks That Equipment Is Properly Set Up.

a. Check for correct line power (115 vac, 50-60 cps).

b. Check that all rear connectors are secure and electrically sound.

NOTE

Although widely used in the electronics industry, the BNC type coaxial connector is only as reliable as the skill and care used to assemble it. Check all connectors carefully and thoroughly.

c. Check that the counter and the functional plug-in are correctly installed.

d. Determine that the input signal (TFM-type plug-in) falls within the requirements for the plug-in. (Refer to Plug-In Instruction Manual.)

e. Check that the input signal is being properly applied to J12, the TFM INPUT jack.

NOTE

The BNC jack marked EXT INPUT located at the front panel of the frequency/ratio counter is not the correct point to apply the TFM input signal. Refer to Section II for instructions on the use of this EXT INPUT jack.

4.2.2 Functional Operational Checks.

If the checks outlined in paragraph 4.2.1 do not uncover any problem, proceed as follows:

a. Turn the POWER switch to RESET; the fan should operate. Except for the counter, all circuits in the DAT proper and in the functional plug-in are energized in the RESET mode, but the DAT dc-to-frequency circuit is disabled by grounding the output of the operational integrator via a contact on the POWER switch. This places the integrator and its control circuits in the proper "starting" state.

b. Turn the POWER switch to ON. The counter Nixie readout tubes should glow. Self-check the counter (refer to Section II, paragraph 2.2).

c. Set counter to measure FREQUENCY B with a time base of 1 second and a short display time. If a L/LSG plug-in is being used, the counter should now indicate the frequency of the DAT output signal, signal B. Place the L/LSG plug-in in the Manual mode. Select the 10 cps to 2 kc range. If using a TFM plug-in, proceed to step d.

d. Set TFM plug-in RATIO and VERNIER controls fully clockwise and activate the TEST button or switch (refer to Plug-In Instruction Manual). The counter should now indicate the DAT output frequency. Set the counter to measure FREQUENCY A, time base of 1 second. The counter should now indicate the frequency of the TFM internal test oscillator.

NOTE

With a TFM plug-in installed and with no TFM input signal applied to J12, the DAT will produce an erratic output signal. The counter will count sporadically in both the frequency A and B positions. This condition is normal and is caused by noise being amplified and converted to dc in the frequency-to-dc portion of the DAT.

In accomplishing the steps listed above, any major malfunction in the counter, the DAT proper, or the functional plug-in will have been uncovered. The following section contains a more detailed trouble shooting procedure to be followed if the above instructions do not reveal the source of difficulty.

4.3 DETAILED TROUBLE SHOOTING PROCEDURE

Refer to the following illustrations, schematics and block diagrams for assistance in trouble shooting the DAT.

Detailed Block Diagram, DAT - TFM Mode	Figure 13
Detailed Block Diagram, DAT - L/LSG Mode	Figure 14
Schematic, Circuit Card A8 (Assy No. 22042-1)	Figure 16
Schematic, Circuit Card A9 (Assy No. 22041-1)	Figure 17

Schematic, Circuit Card A10 (Assy No. 22040-1)	Figure 18
Schematic, Circuit Card A13 (Assy No. 22039-1)	Figure 19
Top View, DAT	Figure 4
Top View, DAT (Partial)	Figure 5
Bottom View, DAT	Figure 6
Interconnecting Diagram, DAT	Figure 11

Figures 7 through 10 show the location of all components on the printed circuit cards noted above.

Amplifiers A1, A2, and A3 are not considered to be field-repairable, and schematic information is not given. Pin connections are printed on the side of the amplifier case.

The DAT regulated power supply provides both + and - 15 vdc for all DAT circuits except the frequency/ratio counter. Figure 15 shows the schematic diagram for this supply. The circuitry used is conventional and may be repaired using standard techniques and tools.

The frequency/ratio counter has its own low and high voltage dc power supplies. The counter is completely independent of the DAT except for ac line power and signal monitoring connections. The DAT will operate normally in all respects with the counter removed. A separate section of this manual contains complete schematic diagrams and trouble shooting information for the counter.

4.3.1 Localizing The Trouble Area

All important signal tracing test points are accessible from the top of the DAT. Several key circuits can be viewed via the rear connectors. Refer to the detailed block diagram for the DAT in the TFM or L/LSG mode, the schematics for cards A8, A9, A10 and A13, and Figure 5, the partial top view of the DAT, for assistance in locating test points and identifying waveforms.

Turn the DAT on and set controls for normal operation. If using a TFM plug-in, apply a suitable input signal to J12 or actuate the TFM internal test oscillator. Turn TFM plug-in ratio controls fully clockwise. If using a L/LSG plus-in, set it for manual operation on the 10 cps to 2 kc range with the manual frequency control set at approximately mid range (5 turns from either end).

Check the DAT power supply output voltages (see DAT bottom view, Figure 6). They should be within ±20 mv of their nominal value of + and - 15 vdc, measured to circuit ground. See power supply adjustments, paragraph 4.5.

Check for the presence of +vdc (up to approximately 10 volts) at J17, the DC OUTPUT jack, or at TP11. Vary the TFM input signal frequency or, with L/LSG plug-in, the setting of the manual frequency control. The +vdc at J17 or TP 11 should vary accordingly. Correct performance up to this point is a general indication that the frequency-to-dc circuitry of the DAT/TFM combination or the ramp generator circuit of the L/LSG plug-in is working correctly. Amplifier A2 must also be functioning properly to achieve the above results.

All DAT test points are active when using a TFM plug-in. With a L/LSG plug-in the frequency-to-dc portion of the DAT is not utilized. Test points 1, 2, 3, 4, 8, 9 and J1-6 are not used (see detailed block diagram of DAT in L/LSG mode).

Additional information can be obtained by observing waveforms at J18 (TFM only), J14, J15, J16 and J19 (L/LSG only). The waveforms should be as described on the rear of the unit. Missing or distorted signals will help identify the trouble area.

Trouble shooting effort may now be concentrated on the appropriate major circuits of the DAT. Refer to test points shown on the detailed block diagram and corresponding waveforms shown on the schematics for A8, A9, A10 and A13. Once the trouble is localized to a particular card or assembly, normal trouble shooting techniques can be used to find and repair the defect.

Instruction manuals for the functional plug-ins contain detailed trouble shooting information and techniques similar to scope to that presented above for the DAT.

4.4 CALIBRATION

Calibration of the DAT is limited to periodically checking the accuracy of the 100 kc clock oscillator in the frequency/ratio counter. This procedure is described in the counter instruction manual.

Procedures for adjusting amplifiers A1, A2, and A3 and for aligning ratio and frequency ranges are given in the instruction manuals for the various functional plug-ins.

4.5 ADJUSTMENT OF POWER SUPPLY VOLTAGES

The power supply produces two regulated voltages, + and - 15 vdc, measured to circuit ground. Two adjustments on the top-front side of the supply control these voltages.

Measure the two voltages at the output terminals on the bottom of the supply (Figure 6). Use a digital voltmeter, a differential voltmeter or other highly accurate and readable instrument. Adjust the potentiometer labeled ADJUST BOTH OUTPUTS (Figure 5) to set the -15 volt output to -15 volts ±20 mv. Adjust the potentiometer labeled ADJUST POS. OUTPUT ONLY to set the +15 volt output to +15 volts ±20 mv.

The plus and minus outputs should have less than 5 millivolts peak-to-peak of combined noise and ripple.

4.6 ADJUSTMENT OF THE SINE SHAPER NETWORK

The sine wave output at connector J14 should contain less than 1% total harmonic distortion over the frequency range of 1 cps to 30 kc. Adjustment of the sine shaper network is required if this specification is not met.

Refer to Section III, Theory of Operation, for a discussion of sine shaper operation. The "breakover" points on the sine waveform may be misleading when attempting to estimate the amount of distortion by visual means. Before making any adjustment of the sine shaper network, measure the total harmonic distortion using a distortion analyzer such as the Hewlett-Packard Model 330B, C or D. If it is greater than 1%, proceed with the following adjustments.

NOTE

Perform the following adjustments with a L/LSG plug-in installed in the DAT if this unit is available.

a. Perform the complete amplifier calibration procedure given in the instruction manual for the functional plug-in being used.

b. Adjust controls on plug-in for a signal B of approximately 1 kc. (Refer to Section II, paragraph 2.4.1 for counter frequency measurement procedure.) Set L/LSG plug-in for manual operation in the 10 cps to 2 kc range. Adjust frequency control as required.

With TFM plug-in, apply a suitable input signal to J12 and adjust ratio controls as required.

c. Connect signal B sine wave output, J14, to the AF INPUT of a Hewlett-Packard Model 330B, C or D distortion analyzer.

d. Connect one input of a dual trace oscilloscope to signal B at the AF INPUT jack of the distortion analyzer.

e. Connect the other oscilloscope input channel to the distortion analyzer jacks marked OUTPUT TO OSCILLOSCOPE.

f. Place oscilloscope in the alternate sweep mode. Trigger the sweep externally by connecting a lead between the distortion analyzer AF INPUT jack and the appropriate external trigger jack on the scope. Set the scope trigger controls for external trigger operation.

g. Referring to the distortion analyzer operating manual for the correct procedure, measure the total harmonic distortion present in signal B. After the proper null has been obtained, adjust the oscilloscope vertical amplifier controls to allow both input signals to be properly displayed. Adjust the oscilloscope time base to display two full cycles of signal B.

At null, the distortion analyzer OUTPUT TO OSCILLOSCOPE signal shows the distortion components remaining in the DAT sine wave output signal. Displaying both signals simultaneously allows the operator to see where the distortion is occurring in the sine wave. The adjustments described in step g will change the waveform and amplitude of the OUTPUT TO OSCILLOSCOPE signal. The lowest total harmonic distortion is obtained when the peak-to-peak amplitude and overall unbalance of this signal have been minimized.

h. Locate SINE SHAPER ADJ potentiometers R12, R20 and R26 on card A8 (figure 7). These potentiometers control the position of the first, second and third "breaks" in the waveform above and below axis crossing, in that order. Carefully adjust R12, R20 and R26 on card A8 to minimize the total harmonic distortion. When a null has been reached, carefully adjust SYMMETRY ADJ potentiometer R12 on card A9 in an attempt to better the null.

NOTE

This last adjustment will change the frequency of signal B and will require a slight retuning of the distortion analyzer.

Continue adjusting R12, R20 and R26 on card A8 and R12 on card A9 until the total harmonic distortion is less than 1%. Remember to re-null the distortion analyzer whenever R12 on card A9 is adjusted.

Final adjustments must be performed using the meter indication on the distortion analyzer. Do not rely on visual examination of the oscilloscope trace to judge the quality of signal B.

4.7 CLEANING

Using low-pressure dry air, a vacuum cleaner, or a soft bristled brush, periodically remove accumulated dust from the DAT chassis and plug-in units.

SECTION V

REPLACEABLE PARTS

5.1 GENERAL

Standard components have been used in this instrument whenever possible. Special components may be obtained direct from the factory. Orders for components should include a complete description of the part, reference designation and part number, along with the model and serial number of the equipment.

Table 5.1 lists certain replaceable components, complete with reference designation, description and part number information, that should be ordered directly from Spectral Dynamics Corporation of San Diego to ensure complete compatibility.

Table 5.1. Replaceable Parts

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER/ MFR. DESIGNATION
Q3A & Q3B; Q4A & Q4B; Q5A & Q5B; Q6A & Q6B on Circuit Card Assembly 22042-1(A8). Q7A & Q7B on Circuit Card Assembly 22040-1(A10).	Transistor, Matched Pair (2N1304 & 2N1305)	2008-211
Q1, Q3, Q5, Q7 and Q8 on Circuit Card Assembly 22041-1(A9). Q5 on Circuit Card Assembly 22040-1(A10).	Transistor, (320)	2008-206
Q3 & Q4 on Circuit Card Assembly 22040-1(A10).	Transistor, (320A)	20008-207
Q2, Q4 and Q6 on Circuit Card Assembly 22041-1(A9). Q2 on Circuit Card Assembly 22040-1(A10).	Transistor, (410)	20008-208

Table 5.1. Replaceable Parts (Continued)

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER/ MFR. DESIGNATION
A8	Printed Circuit Card Assembly	22042-1
A9	Printed Circuit Card Assembly	22041-1
A10	Printed Circuit Card Assembly	22040-1
A13	Printed Circuit Card Assembly	22039-1
A1, A2 and A3	Amplifier	Philbrick P65A
A11	Power Supply	AC-DC TP15D2-2
A12	Fan	Rotron Grille Fan
A5	Counter, Freq/Ratio	20013-014
S1	Switch, Power	Grayhill 5003-3-S

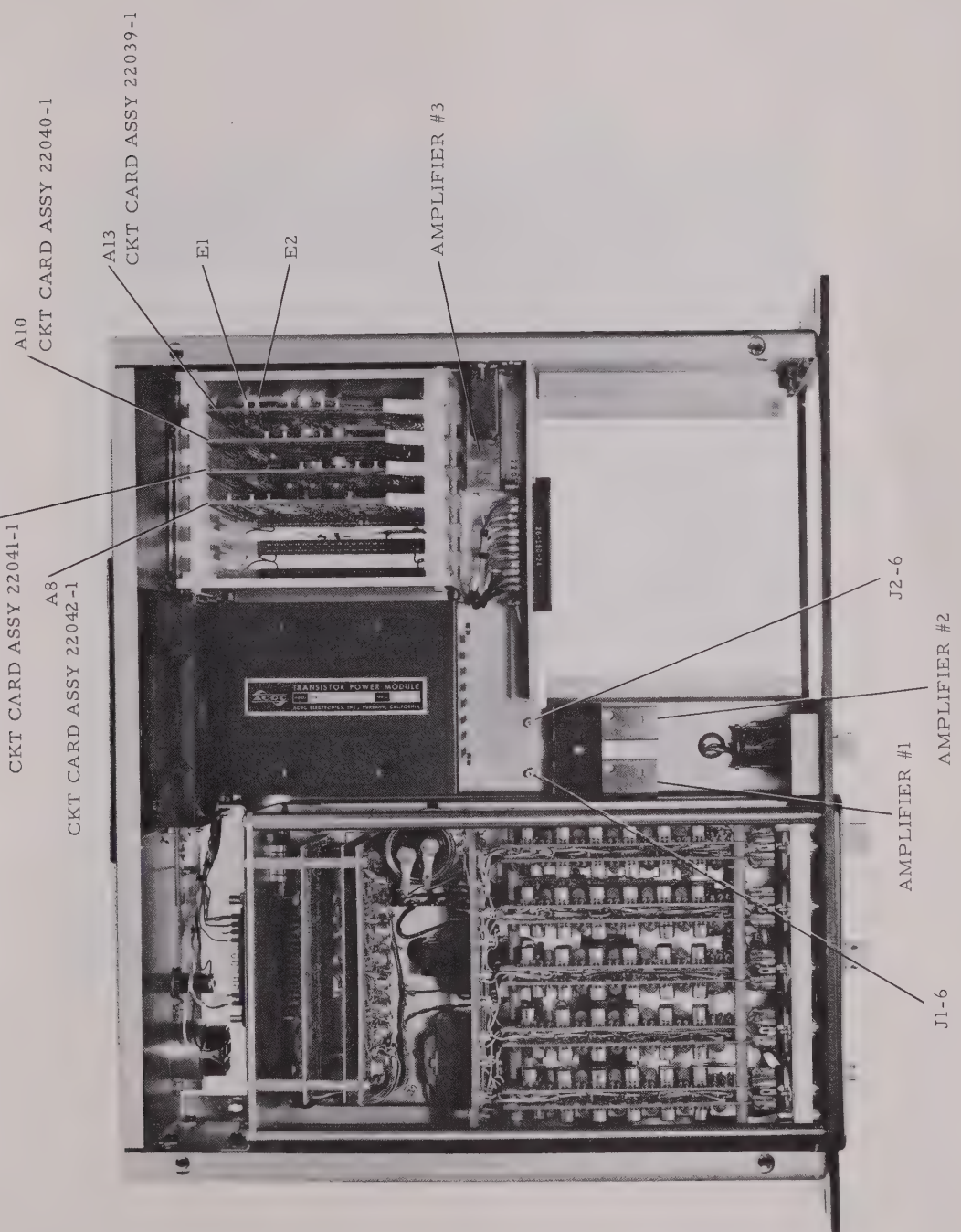


Figure 4. Top View

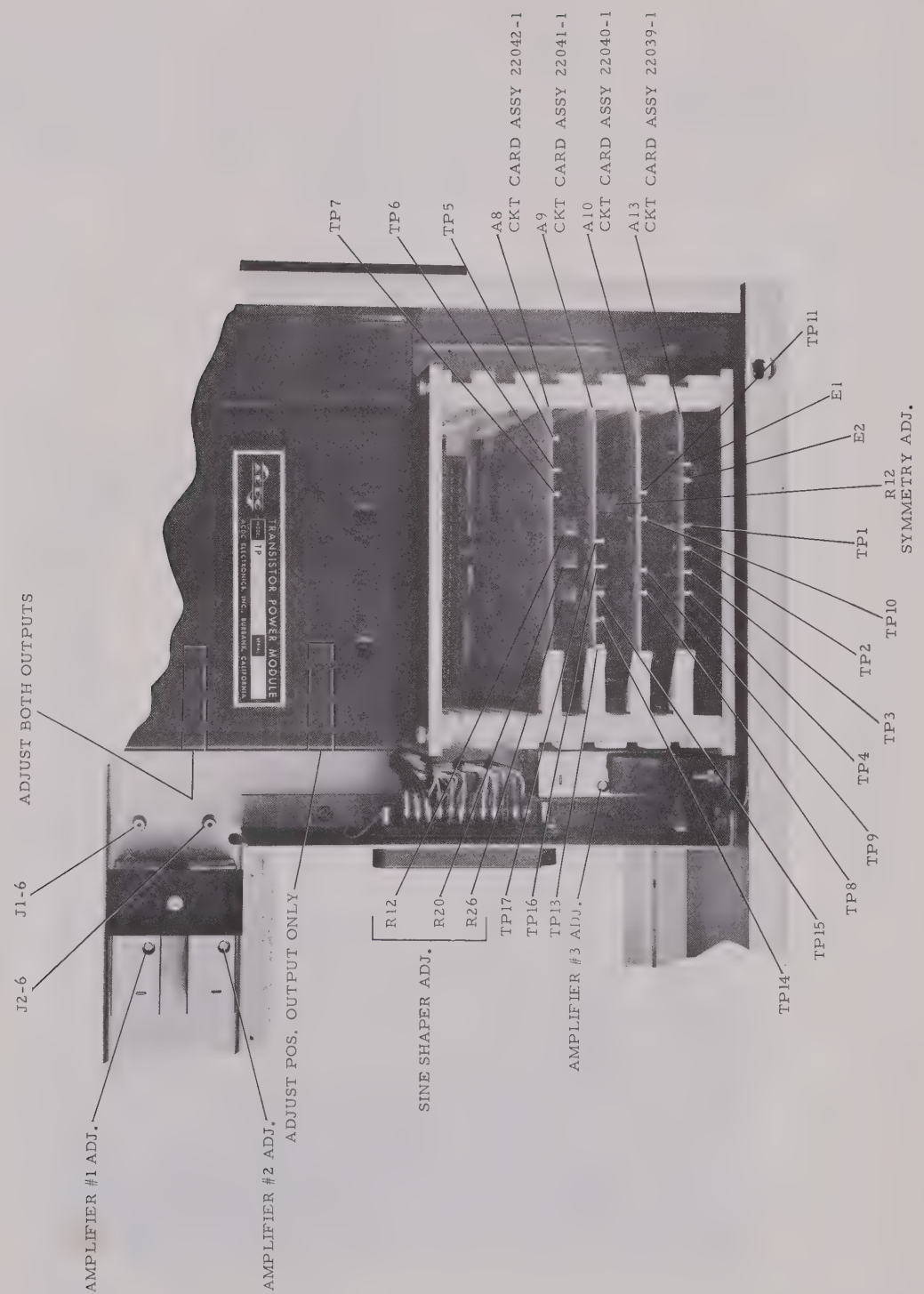


Figure 5. Partial Top View

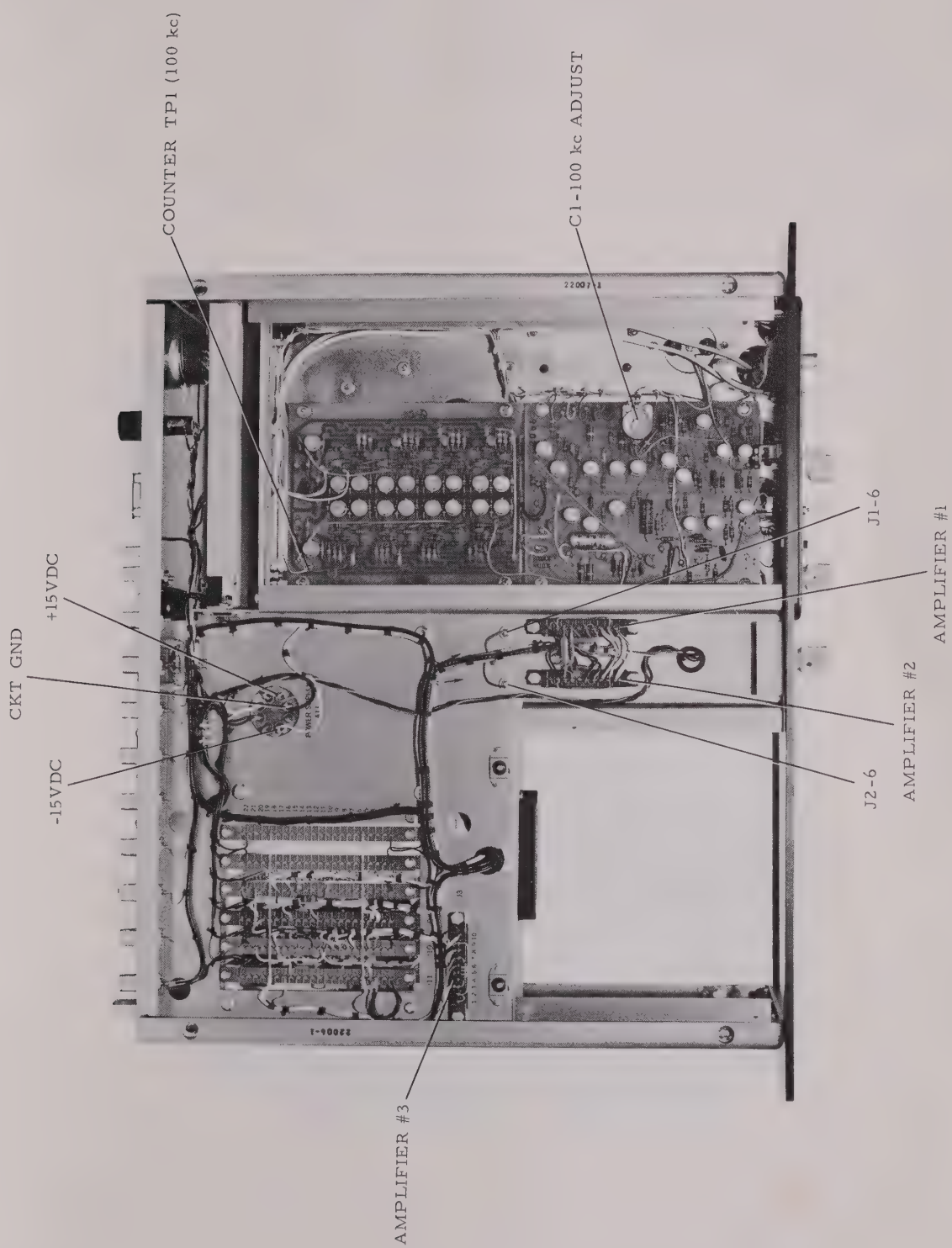


Figure 6. Bottom View

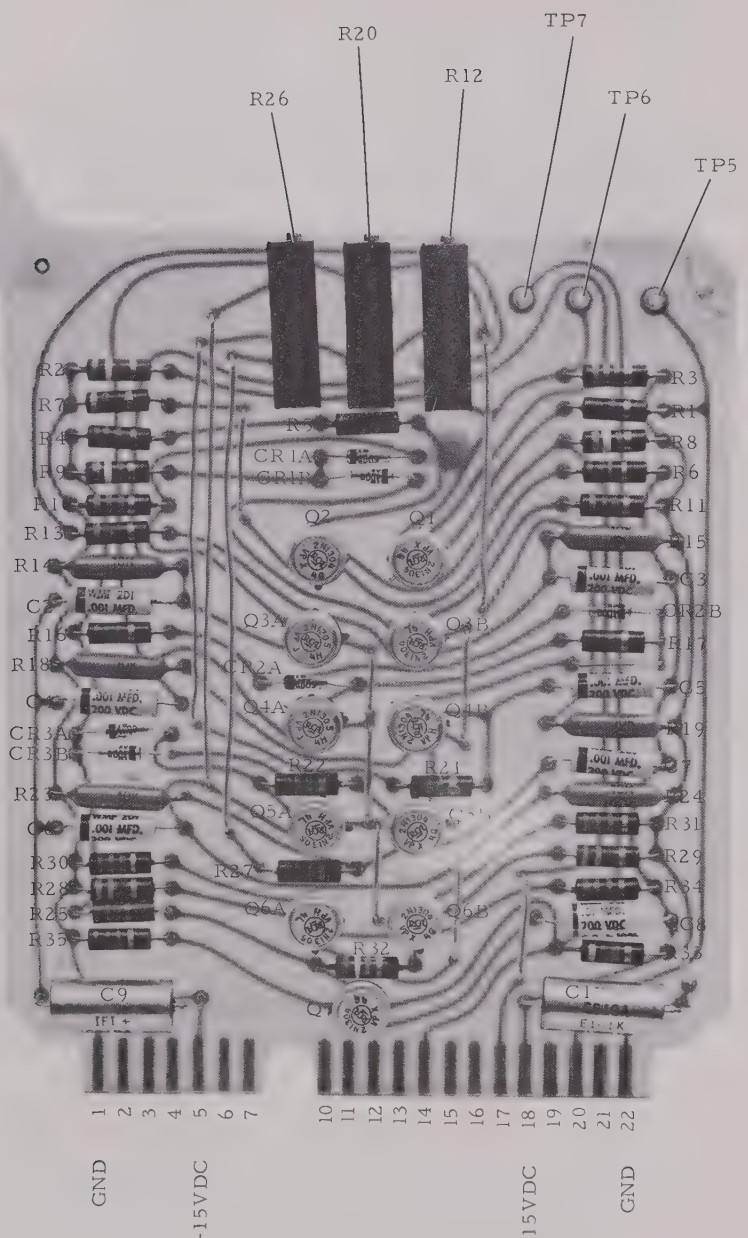


Figure 7. Component Locations on Circuit Card Assembly No. 22042-1 (A8)

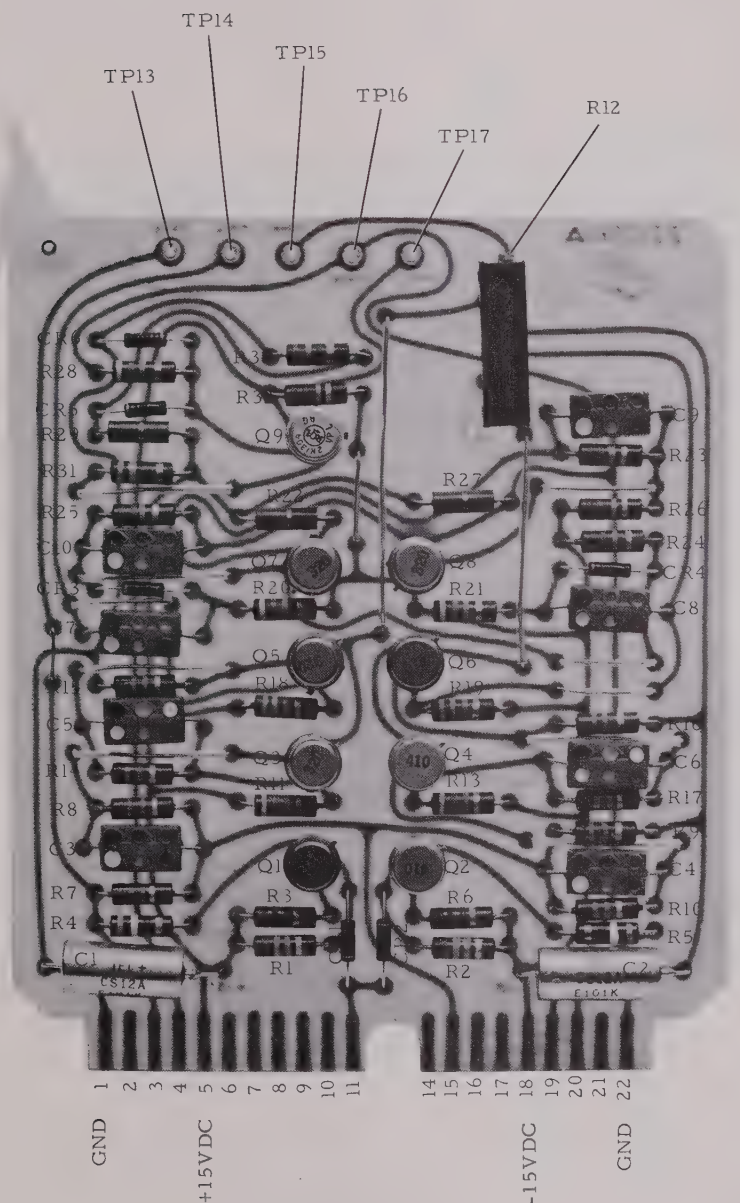


Figure 8. Component Locations on Circuit Card Assembly No. 22041-1 (A9)

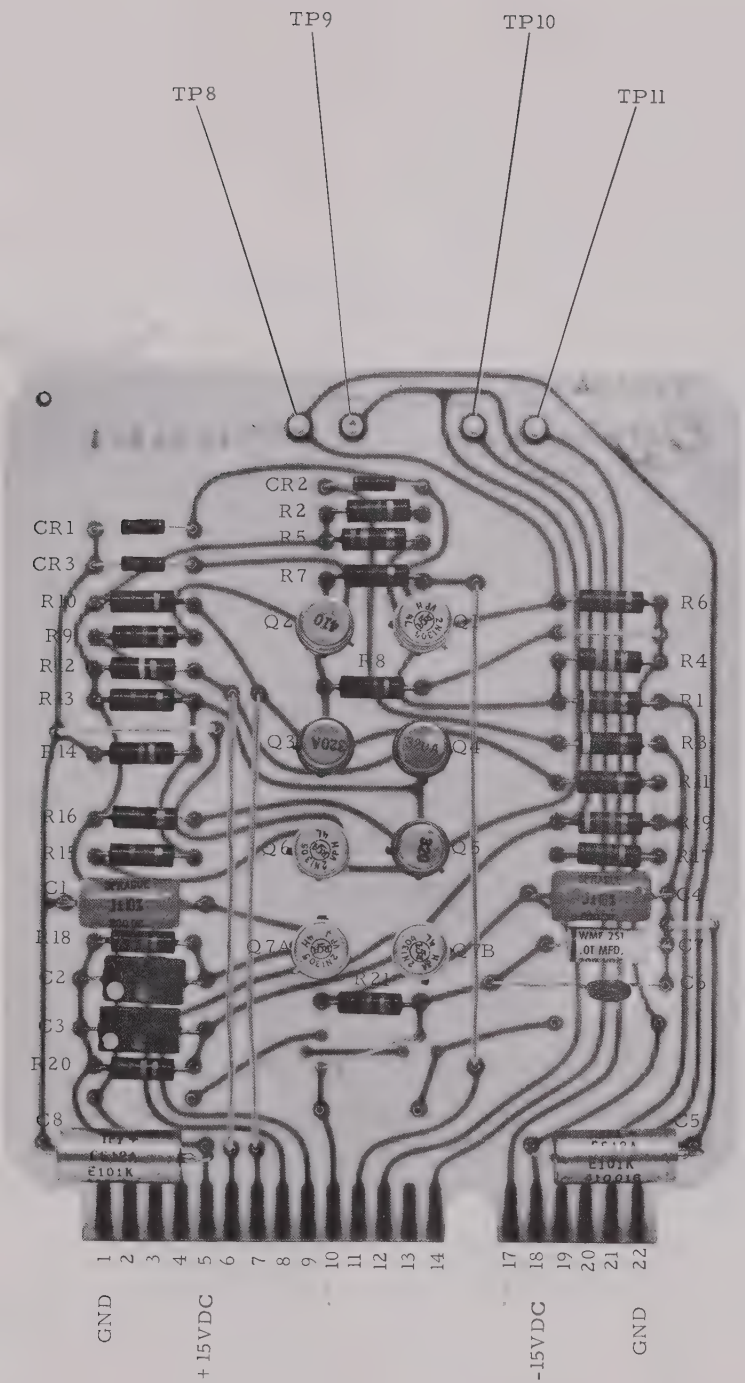


Figure 9. Component Locations on Circuit Card Assembly No. 22040-1 (A10)

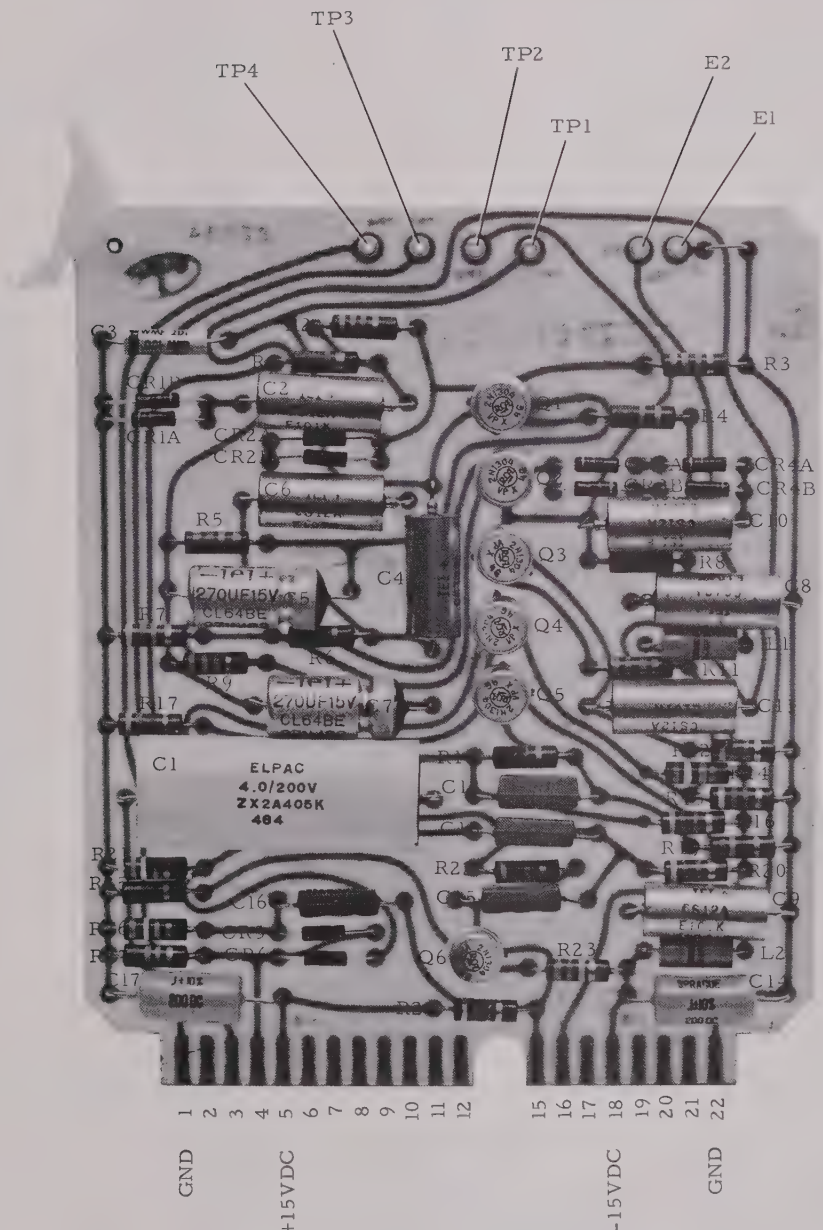
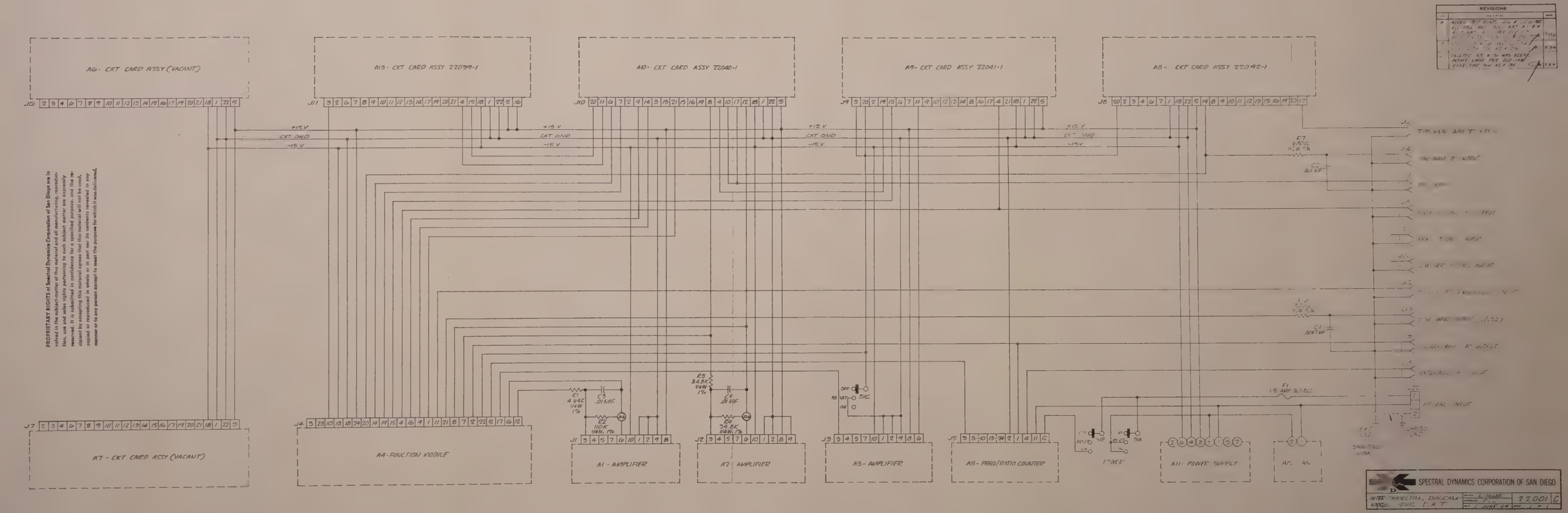
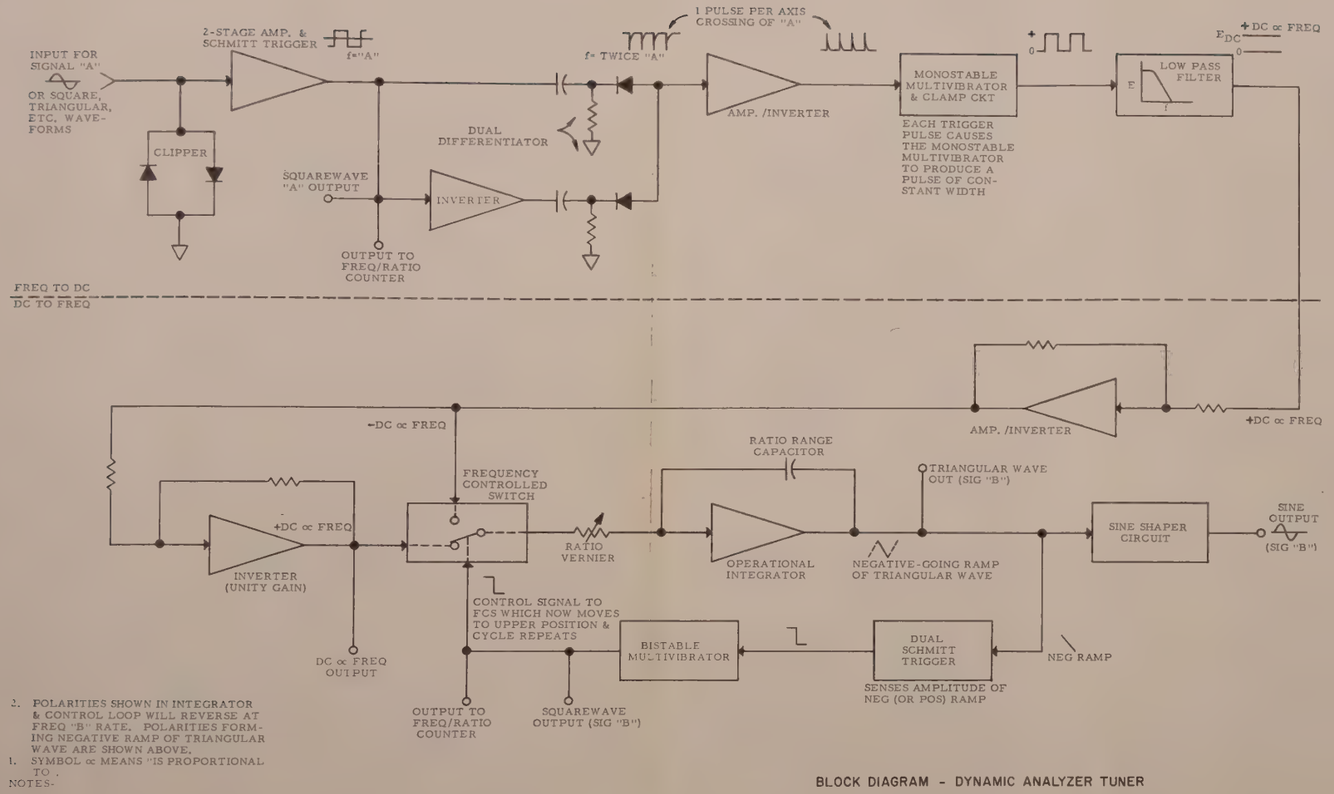


Figure 10. Component Locations on Circuit Card Assembly No. 22039-1 (A13)



PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

▲ Figure 11. Interconnecting Diagram


INPUT FOR SIGNAL "A"
OR SQUARE, TRIANGULAR, ETC. WAVE-FORMS
2-STAGE AMP. & SCHMITT TRIGGER
f="A"
CLIPPER
SQUAREWAVE "A" OUTPUT
OUTPUT TO FREQ/RATIO COUNTER
DUAL DIFFERENTIATOR
INVERTER
f= TWICE "A"
1 PULSE PER AXIS CROSSING OF "A"
AMP. /INVERTER
MONOSTABLE MULTIVIBRATOR & CLAMP CKT
EACH TRIGGER PULSE CAUSES THE MONOSTABLE MULTIVIBRATOR TO PRODUCE A PULSE OF CONSTANT WIDTH
LOW PASS FILTER
+DC ∝ FREQ
FREQ TO DC
DC TO FREQ
AMP. /INVERTER
+DC ∝ FREQ
-DC ∝ FREQ
RATIO RANGE CAPACITOR
TRIANGULAR WAVE OUT (SIG "B")
FREQUENCY CONTROLLED SWITCH
+DC ∝ FREQ
INVERTER (UNITY GAIN)
RATIO VERNIER
OPERATIONAL INTEGRATOR
NEGATIVE-GOING RAMP OF TRIANGULAR WAVE
SINE SHAPER CIRCUIT
SINE OUTPUT (SIG "B")
CONTROL SIGNAL TO FCS WHICH NOW MOVES TO UPPER POSITION & CYCLE REPEATS
BISTABLE MULTIVIBRATOR
DUAL SCHMITT TRIGGER
NEG RAMP
SENSES AMPLITUDE OF NEG (OR POS) RAMP
DC ∝ FREQ OUTPUT
OUTPUT TO FREQ/RATIO COUNTER
SQUAREWAVE OUTPUT (SIG "B")
2. POLARITIES SHOWN IN INTEGRATOR & CONTROL LOOP WILL REVERSE AT FREQ "B" RATE. POLARITIES FORMING NEGATIVE RAMP OF TRIANGULAR WAVE ARE SHOWN ABOVE.
1. SYMBOL ∝ MEANS "IS PROPORTIONAL TO".
NOTES-

BLOCK DIAGRAM - DYNAMIC ANALYZER TUNER

Figure 12. Block Diagram

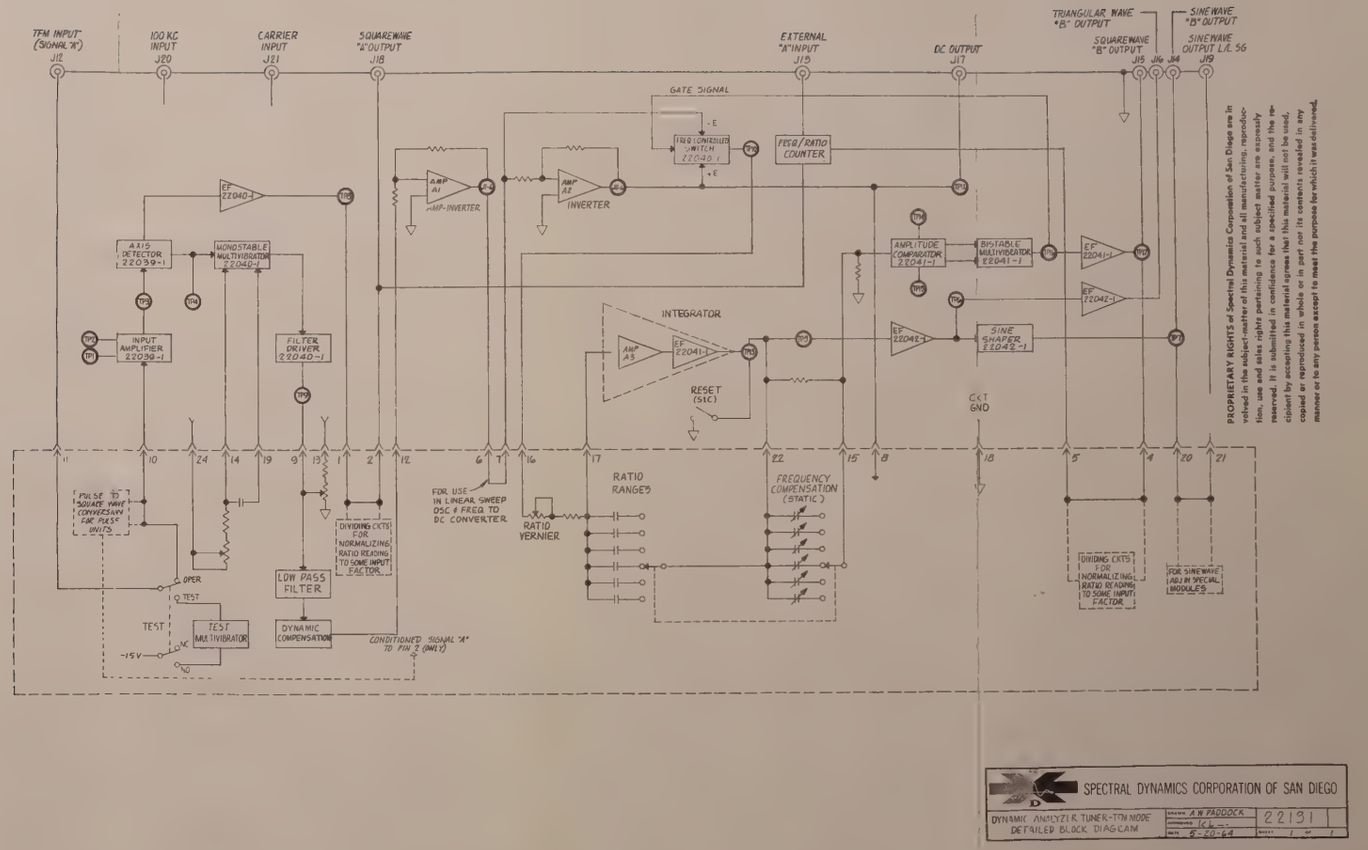
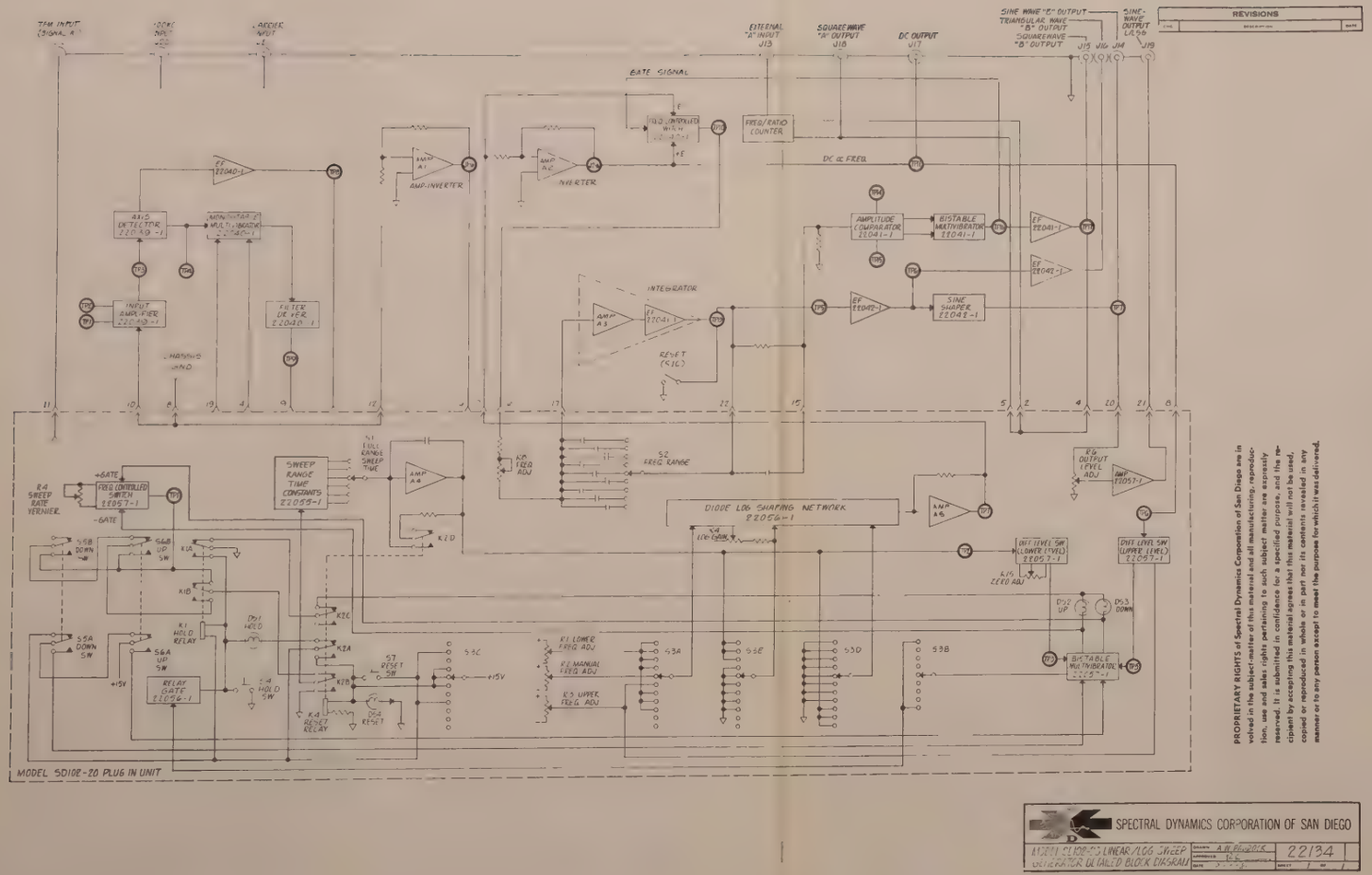

TFM INPUT (SIGNAL "A") J12
100 KC INPUT J20
CARRIER INPUT J21
SQUAREWAVE "A" OUTPUT J18
EXTERNAL "A" INPUT J15
DC OUTPUT J17
TRIANGULAR WAVE "B" OUTPUT
SQUAREWAVE "B" OUTPUT J16
SINEWAVE "B" OUTPUT J46
SINEWAVE OUTPUT LVL 56 J19
GATE SIGNAL
FREQ CONTROLLED SWITCH 22040-1
FREQ/RATIO COUNTER
EF 22040-1
AMP A1 -AMP-INVERTER
AMP A1 INVERTER
AXIS DETECTOR 22039-1
MONOSTABLE MULTIVIBRATOR 22040-1
INPUT AMPLIFIER 22039-1
FILTER DRIVER 22040-1
INTEGRATOR
AMP A3
EF 22041
RESET (S1C)
AMPLITUDE COMPARATOR 22041-1
BISTABLE MULTIVIBRATOR 22041-1
EF 22041-1
EF 22042-1
EF 22043-1
SINE SHAPER 22042-1
CKT GND
PULSE TO SQUARE WAVE CONVERSION FOR PASS UNITS
OPER
TEST
TEST MULTIVIBRATOR
-15V
LOW PASS FILTER
DYNAMIC COMPENSATION
CONDITIONED SIGNAL "A" TO PIN 2 (ONLY)
DIVIDING CKTS FOR NORMALIZING RATIO READING TO SOME INPUT FACTOR
FOR USE IN LINEAR SWEEP OSC'S FREQ TO DC CONVERTER
RATIO VERNIER
RATIO RANGES
FREQUENCY COMPENSATION (STATIC)
DIVIDING CKTS FOR NORMALIZING RATIO READING TO SOME INPUT FACTOR
FOR SINEWAVE ADJ IN SPECIAL MODULES
PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.
SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO
DYNAMIC ANALYZER TUNER-TFM MODE DETAILED BLOCK DIAGRAM
DRAWN A.N. PADDOCK
APPROVED
DATE 8-20-64
22131

Figure 13. Dynamic Analyzer Tuner - TFM Mode Detailed Block Diagram



PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

MODEL SD10E-20 LINEAR/LOG SWEEP GENERATOR DETAILED BLOCK DIAGRAM

DRAWN A. WILBOURN 22134

APPROVED

DATE 5-1-73

SHEET 1 OF 1

Figure 14. Linear/Log Sweep Generator Detailed Block Diagram

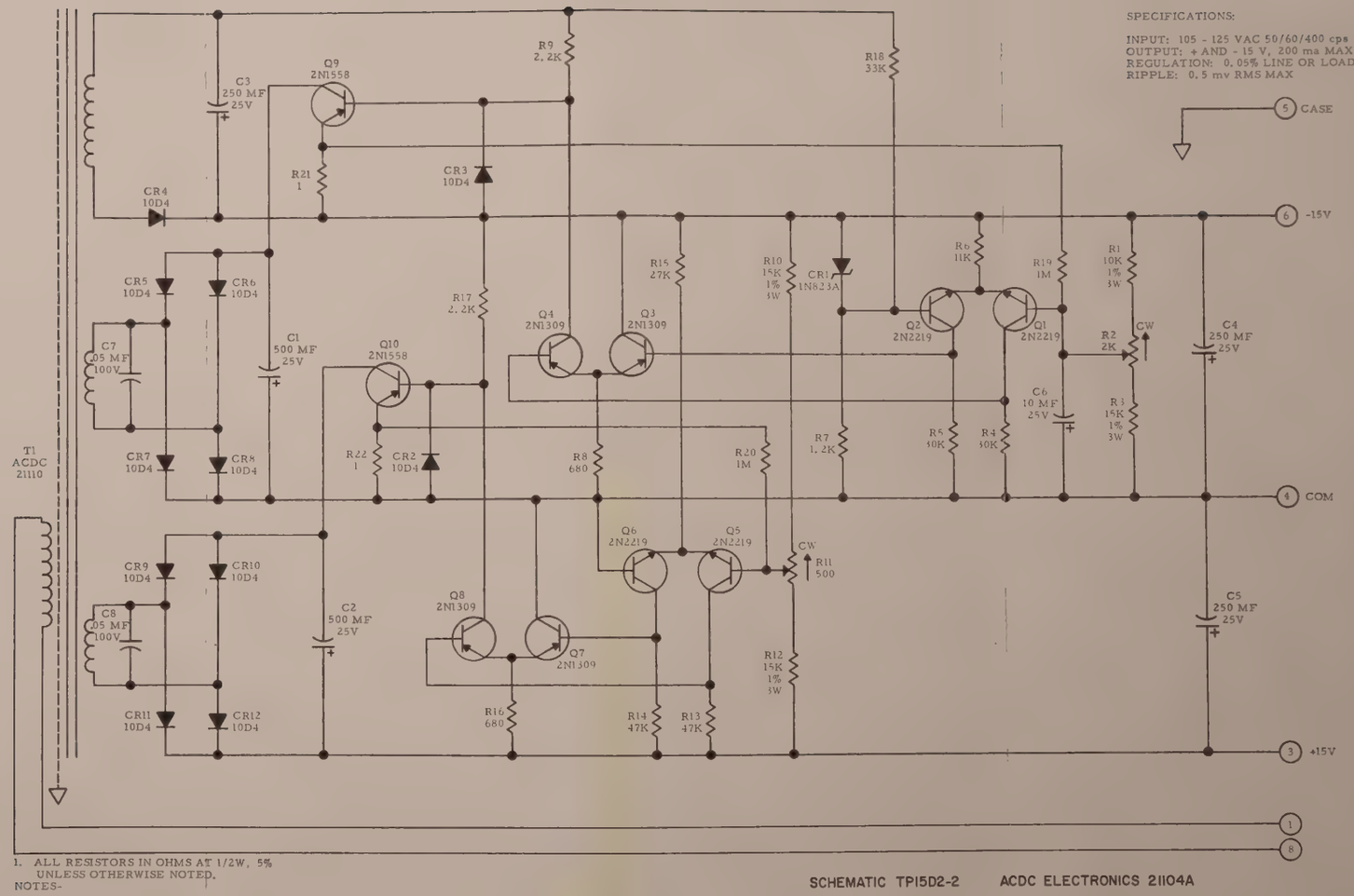
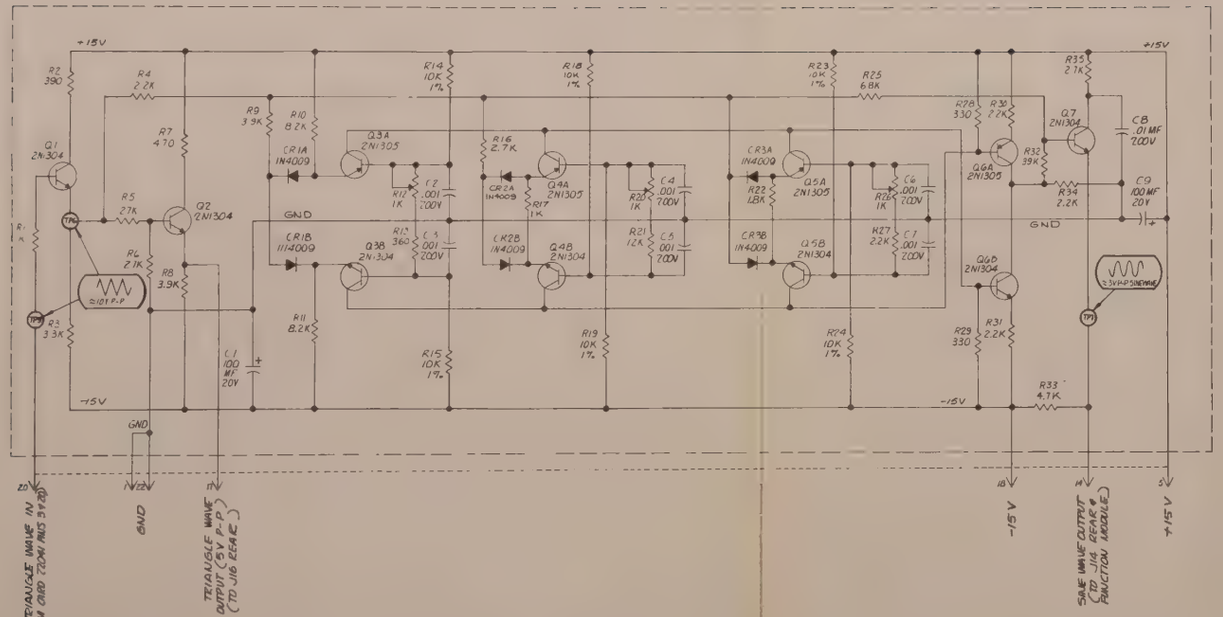


Figure 15. Power Supply Schematic Diagram

PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

REVISIONS		
LTR	DESCRIPTION	DATE
A	PRODUCTION RELEASE FOR SAI 11 & DU R.P.	15 MAR



3. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS AT 1/2 W, ±5%.
2. THE FOLLOWING CONNECTOR PINS ARE SPARES 2-4, 6-13, 15, 16, 19 & 21.
1. SEE 22037-1 FOR PRINTED CIRCUIT DETAIL.

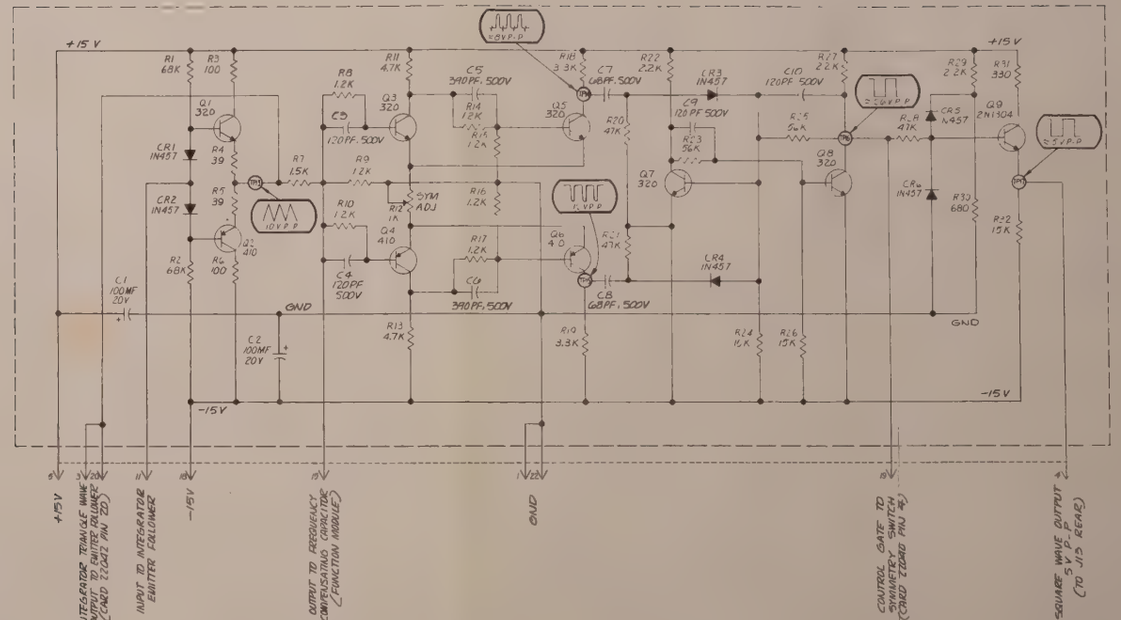
NOTE -

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO			
SCHEMATIC - LIDDEL SD102	DRAWN A. N. MADDOCK	22095	A
CKT CARD ASSY 22042-1	APPROVED		
	DATE 27 MAY 1964	SHEET 1 OF 1	

Figure 16. Circuit Card No. 22042-1 (A8) Schematic Diagram

PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

REVISIONS			
LTR	DESCRIPTION		DATE
A	R-7 WAS 1.2K PER ECO-090. REFLECTS STOP ON 3/N II & ON R RETRO		



3. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS AT ½ W. ± 5%
2. THE FOLLOWING CONNECTOR PINS ARE SPARES 2, 6-10, 12-14, 16-17 & 21.
1. SEE 22036-1 FOR PRINTED CIRCUIT DETAIL.

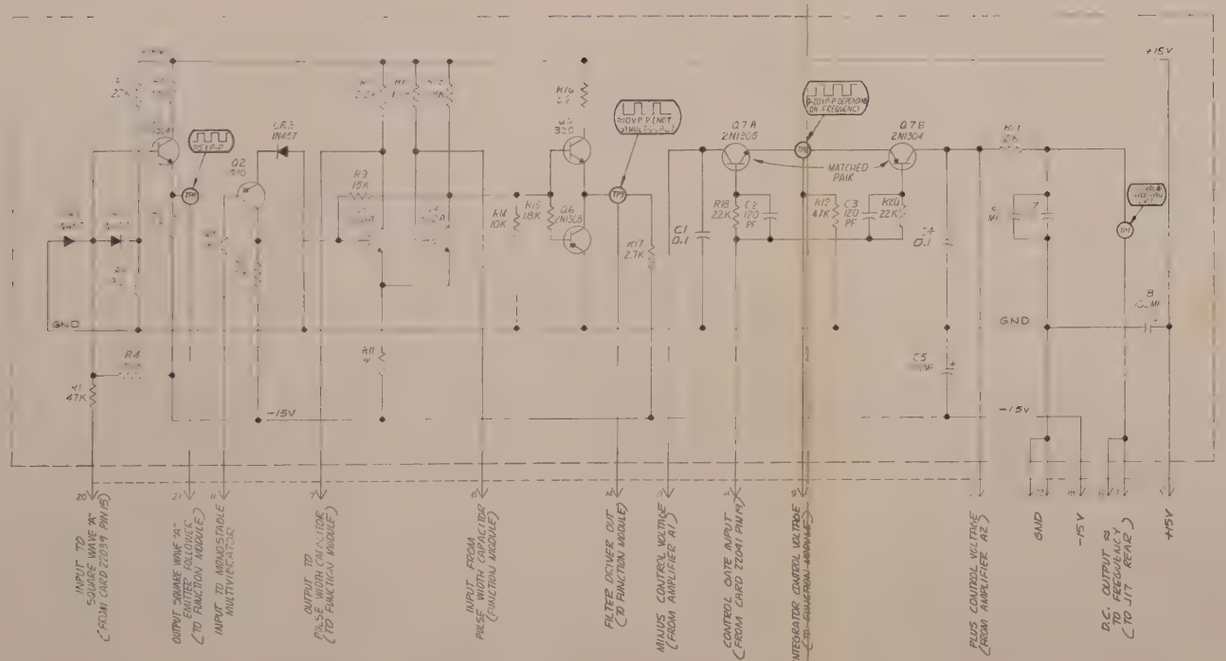
NOTE:

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO			
SCHEMATIC- MODEL SD102 CKT CARD ASSY 22041-1	DRAWN A.M. PADDOCK	22094	A
	DATE 27 MAY 68	SHEET 1 OF 1	

Figure 17. Circuit Card No. 22041-1 (A9) Schematic Diagram

PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

REVISIONS		
LTR	DESCRIPTION	DATE
A	PRODUCTION RELEASE FOR S/N 11 & ON E.P.	8-31-66
C	DELETED R99, R23, Q8, Q9, C104 PER ECO-134. EFFECTIVE S/N 42 & ON.	8-11-66 AP



3. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS AT 1/2W ±5%.
2. THE FOLLOWING CONNECTOR PINS ARE SPARES 2, 3, 13, 15, 16 & 19.
1. SEE 22[illegible] FOR [illegible] IN DETAIL

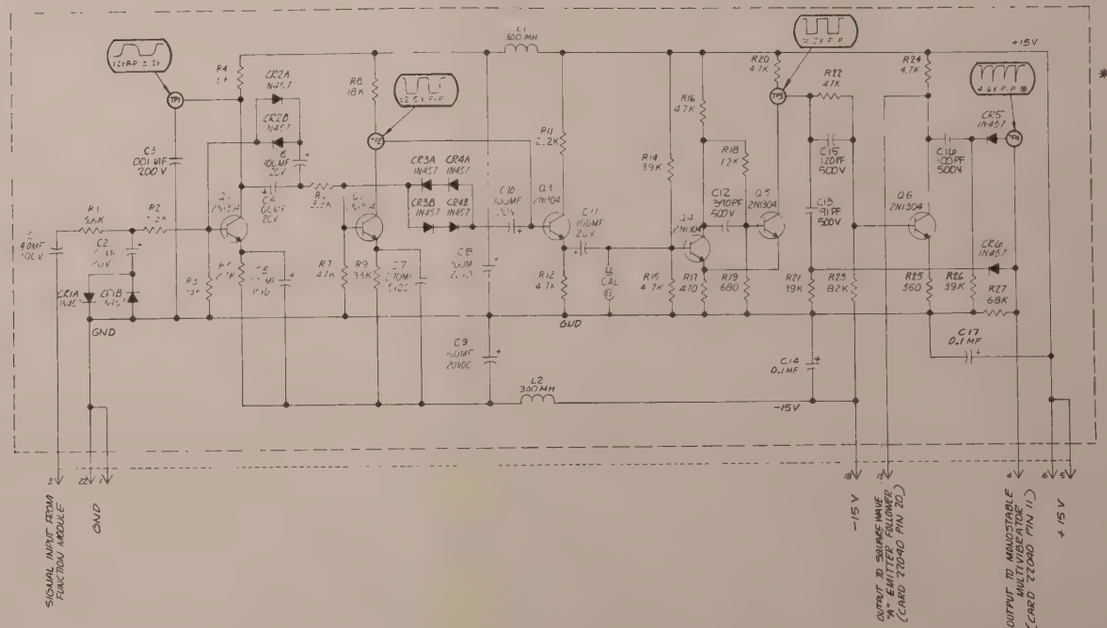
NOT

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO			
SCHEMATIC-MODEL SD1012	DRAWN ALAN FAIRBANK	22093	B
CKT CARD ASSY 22040-1	APPROVED		
	DATE 27 MAY 1966	SHEET 1 OF 1	

Figure 18. Circuit Card No. 22040-1 (A10) Schematic Diagram

PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego are involved in the subject-matter of this material and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose, and the recipient by accepting this material agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

REVISIONS		
LTR	DESCRIPTION	DATE
A	PRODUCTION RELEASE FOR S/N 1160N	5-31-68
B	REVISED SCHEMATIC TO REFLECT MATCHED DIODES. EFFECTIVE S/N 1180N PER ECO-1418. K/MARE	7-19-68



* NOTE - WITH CARD ASSY 22040-1 REMOVED

NOTE -
1. SEE 22039-7 FOR CIRCUIT CARD DETAIL
2. THE FOLLOWING CONNECTOR PINS ARE SPARES 2, 6-14, 17, 19, 20 & 21.
3. UNLESS OTHERWISE STATED ALL RESISTORS ARE IN OHMS AT 1/2W, 5%.

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

SCHEMATIC - LADDER 3 DIOD	DRAWN A.W. MOORE	22072	B
CKT CARD ASSY 22039-1	CHECKED		
	DATE 10 MAY 68	SHEET 1 OF 1	

Figure 19. Circuit Card No. 22039-1 (A13) Schematic Diagram

SERIAL NUMBER _____

Schematic Change Letter _____

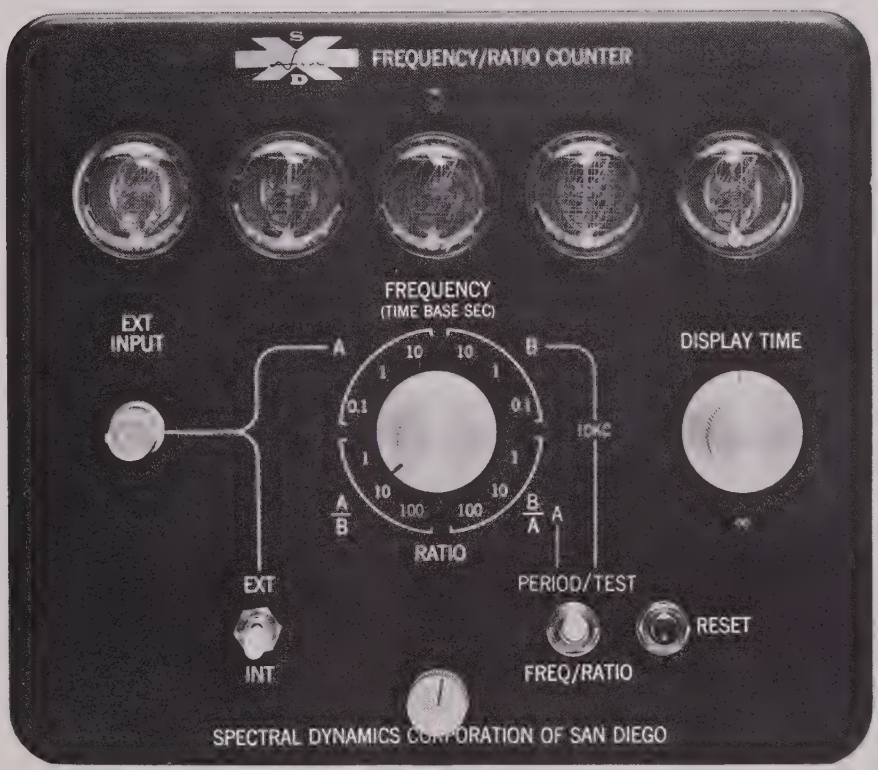
INSTRUCTION MANUAL

FREQUENCY/RATIO COUNTER

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

8159 Engineer Road, P. O. Box 671
San Diego, California 92112
Area Code 714, 278-2501

1 November 1964



Frequency/Ratio Counter Module

TABLE OF CONTENTS

Section			Page
I	GENERAL DESCRIPTION AND SPECIFICATIONS		1
	1.1	General Description	1
	1.2	Specifications	1
II	OPERATIONAL CONTROLS		3
	2.1	Function Selector Switch	3
	2.2	Display Time Knob	3
	2.3	Period/Test - Freq/Ratio Switch	3
	2.4	Reset Pushbutton	3
	2.5	Ext-Int Switch	3
III	BLOCK DIAGRAM DISCUSSION		5
	3.1	General	5
	3.2	Frequency Measurement	7
	3.2.1	Input Signal Flow	7
	3.2.2	Control Logic	7
	3.2.3	Self-Test	8
	3.2.4	Time Base	8
	3.3	Period Measurement	8
	3.3.1	Input Signal Flow	8
	3.3.2	Counting and Logic	10
	3.4	Ratio Measurement	10
	3.4.1	Input Signal Flow	10
	3.4.2	Counting and Logic	10
IV	CIRCUIT DESCRIPTIONS		11
	4.1	Input Amplifier	11
	4.2	Decade Counters	11
	4.2.1	Block Diagram Discussion	11
	4.3	Display Timer	15
	4.4	Reset Pulser	15
	4.5	OR Gate	15
	4.6	Totalizer Gate	15

TABLE OF CONTENTS (CONTINUED)

Section			Page
IV	4.7	100 kc Oscillator	15
	4.8	Decade Scaler	20
	4.9	Reset	20
	4.10	Power Supply	20
V	MAINTENANCE AND CALIBRATION		23
	5.1	Calibration Of 100 kc Oscillator	23
	5.2	Routine Maintenance	23
	5.3	Malfunction and Repair	23
	5.3.1	Recommended Spares	23

LIST OF ILLUSTRATIONS

Figure	Title	Page
1	Frequency Counting - Simplified Block Diagram	6
2	Period Counting - Simplified Block Diagram	6
3	Ratio Measurement - Simplified Block Diagram	7
4	Decade Scaler With Reset - Schematic Diagram	9
5	Input Amplifier Schematic Diagram	12
6	Right Side View - Frequency/Ratio Counter	13
7	Component Locations For Input Amplifier	14
8	Decade Counter Block Diagram	14
9	Toggle Schematic Diagram	16
10	Decade Counter Schematic Diagram	17
11	Control Logic Schematic Diagram	18
12	100 kc Oscillator Schematic Diagram	19
13	Power Supply Schematic Diagram	20
14	Decade Scaler Schematic Diagram	21
15	Component Locations For Decade Scaler	24
16	Bottom View - Frequency/Ratio Counter	25
17	Component Locations For 100 kc Oscillator and Control Logic	26
18	Left Side View Ratio Counter	27
19	Component Locations For Decade Scaler With Reset	28
20	Top View - Frequency/Ratio Counter	29
21	Component Locations For Decade Counter	30
22	Frequency/Ratio Counter Block Diagram	31

SECTION I

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 GENERAL DESCRIPTION

The Frequency/Ratio Counter module is a part of the Spectral Dynamics Corporation Model SD102 Dynamic Analyzer Tuner (DAT).

The Counter measures frequency, ratio and period of signals supplied by the DAT or by an external source. Features of the counter include:

All solid state design
Dual 100 mv rms input amplifiers
Five-digit Nixie readout
Self-test capability
Frequency measurement with 0.1, 1 and 10 second gate times
Period measurement with 1, 10 and 100 period average
Ratio of signals A/B or B/A for 1, 10 and 100 periods .

Line power (105-125 vac, 50/60 cps) and signal inputs are received directly from the DAT via a rear connector, engaged when the counter is correctly installed in the left side of the DAT chassis.

Complete operating instructions for this counter will be found in the SD102 DAT instruction manual.

1.2 SPECIFICATIONS

Input requirements:	Sine wave - 0.1 rms minimum Square wave or pulse - 0.1v p-p minimum
Frequency range:	Sine wave - 3 cps to 100 kc Square wave or pulse - DC to 100 kc
Frequency gate time:	0.1, 1 and 10 seconds
Frequency measurement accuracy:	± 1 count ± time base accuracy
Periods averaged for PERIOD or RATIO:	1, 10 and 100
Period/Ratio measurement accuracy:	± 1 count ± time base accuracy (Period) ± trigger error

Time base:	100 kc crystal controlled oscillator. May be standardized against WWV.
Time base stability:	Aging ± 2 ppm/week, temp. ± 20 ppm 15°C to 40°C
Display:	5 digit Nixie
Display time:	0.2 to 6 seconds, and infinite
Power requirements:	105-125 volts, 50/60 cps, 25 watts

SECTION II

OPERATIONAL CONTROLS

2.1 FUNCTION SELECTOR SWITCH

This switch determines the mode of operation of the counter. Basic settings are for the frequency of input signals A or B and the ratio of A/B or B/A.

2.2 DISPLAY TIME KNOB

This knob permits control over the counter display time on all Function Selector switch positions. The display time can be varied from approximately 0.2 seconds minimum to 6 seconds maximum, with infinite hold available by turning the knob fully counterclockwise.

2.3 PERIOD/TEST - FREQ/RATIO SWITCH

With this switch in the FREQ/RATIO position the Function Selector switch determines the mode of operation of the counter (see paragraph 2.1).

With the switch in the PERIOD/TEST position a 10 kc signal from the counter time-base section is applied to the totalizer gate. Depending on the setting of the Function Selector switch, the counter will now self-check its decade counters (totalizer section) or measure the period of input signal A.

2.4 RESET PUSHBUTTON

This pushbutton permits manual reset of the totalizer section (Nixie readout) at any time during counter operation.

2.5 EXT - INT SWITCH

This switch enables the operator to connect an external signal (100 mv rms minimum) to the A input amplifier. This is a convenience feature allowing measurement of the frequency or period of signals not related to the DAT operation. The ratio of the external A signal to the DAT-supplied B signal is read with the Function Selector switch in the appropriate ratio position.

SECTION III

BLOCK DIAGRAM DISCUSSION

3.1 GENERAL

The Frequency/Ratio counter can be described as having four basic elements (see Figure 22):

Totalizer
Totalizer Gate
Time Base Generator (clock)
Logic Circuit

The totalizer consists of five decade counter modules connected in cascade. A Nixie-type indicator tube is used as an active element of each counter module and displays the count held by the module. A pulse applied to the totalizer advances the count of the first (units) counter by one numeral. Each time the number on the first counter is advanced from 9 to 0 it puts out a pulse which advances the count on the second (tens) counter by one number, and so on through all five counters.

The totalizer gate responds to commands from the logic circuit and starts and stops the flow of input signals to the totalizer.

The time base generator is a precision crystal controlled clock producing accurate timing signals for use by the counter.

The logic circuit controls the overall counter operation, determining when the totalizer gate should open and shut, holding the display for a convenient time, and resetting all circuit elements prior to starting a new measurement.

To measure frequency the logic circuit opens the totalizer gate and allows the totalizer to count cycles of the input signal for a precise length of time. The time base generator supplies the timing information. At the end of the time period the logic circuit closes the gate, blocking the input signal from the totalizer. The operator then reads the count shown on the totalizer display and interprets it as cycles per unit time (example: cycles per second).

The logic circuit resets (clears) the totalizer prior to the start of a new count.

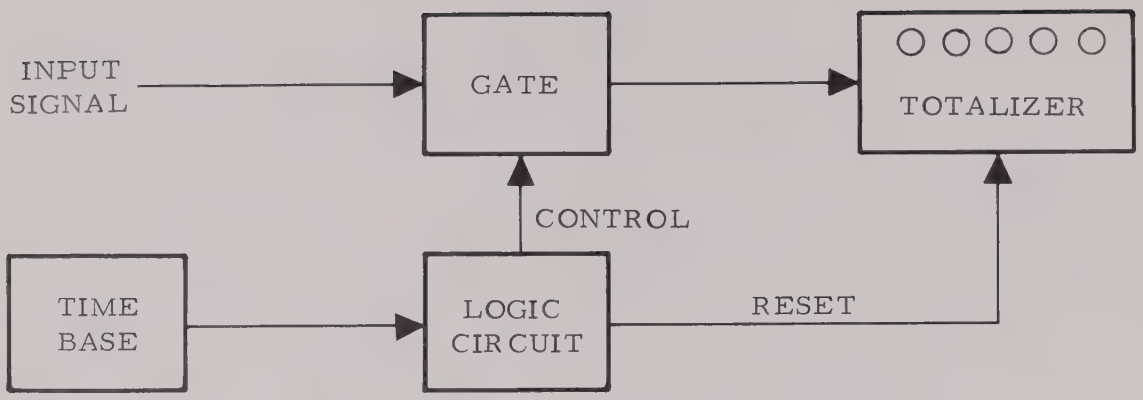


Figure 1. Frequency Counting - Simplified Block Diagram

Period (the reciprocal of frequency) is the time required for one cycle of a signal to occur. The counter measures the period of the input signal by using the signal to control the totalizer gate, opening the gate and then closing it exactly one cycle later. While open the gate allows pulses from the time base section to pass to the totalizer and be counted. The totalizer display can be read directly in units of time, giving the period of the input signal.

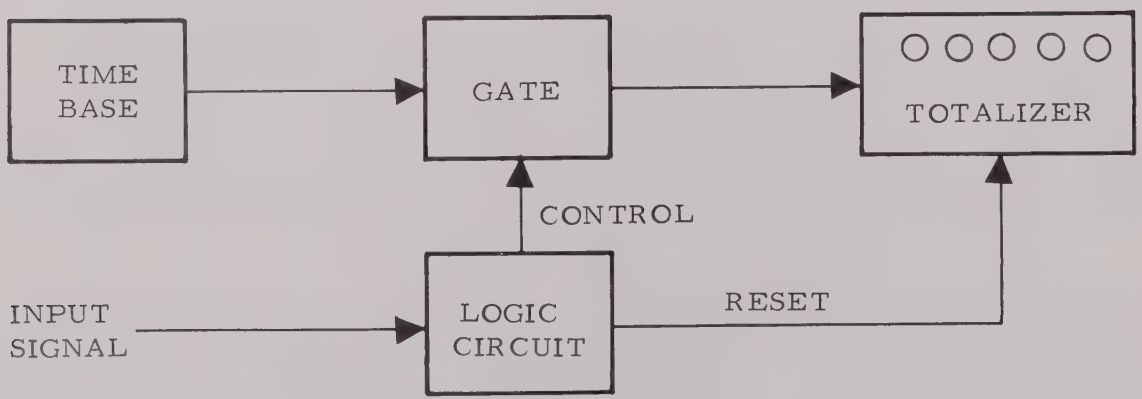


Figure 2. Period Counting - Simplified Block Diagram

The frequency ratio between two signals is the number of cycles of the higher frequency signal that occur during one cycle of the lower frequency signal. Example: If 86 cycles of signal A occur during 1 cycle of signal B, the ratio of A to B is 86 to 1.

To measure the frequency ratio between two signals the counter uses the lowest frequency signal to control the totalizer gate. The gate opens for one cycle of this signal. While open the gate allows the totalizer to count cycles of the higher frequency signal. Therefore after the gate closes the totalizer display gives the number of cycles of the higher frequency that occurred during one cycle of the lower frequency ratio between the two signals.

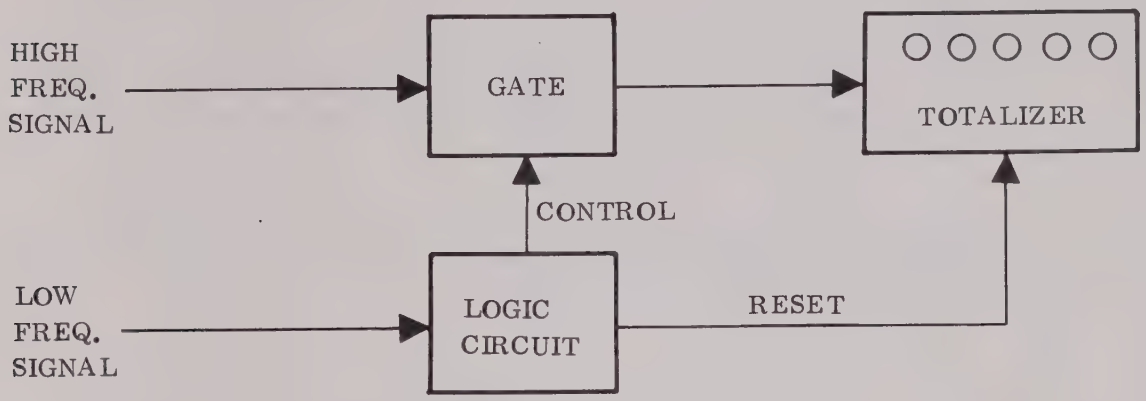


Figure 3. Ratio Measurement - Simplified Block Diagram

3.2 FREQUENCY MEASUREMENT

3.2.1 Input Signal Flow

Identical input amplifiers condition signals A and B into fast rise-time pulses or square waves (depending on the symmetry of the input signals). Signal A passes directly to the Function Selector switch. Signal B goes to the FREQ/RATIO - PERIOD/TEST switch (hereafter called F/R-P/T switch), then to the Function Selector switch.

The Function Selector switch connects the desired signal to the Totalizer Gate and Pulse Shaper. The signal passes through this gate to the counter only when the gate is opened by a suitable gate control signal. The gated and shaped input signal is counted in the totalizer and the accumulated total is displayed by the Nixie tubes.

3.2.2 Control Logic

If one of the frequency settings is made (0.1, 1, or 10 SECONDS), the control logic signal flow begins at the display timer. A signal from the selected time base (10 cps, 1 cps, or 0.1 cps) trips the display timer, the output of which (through the OR gate) controls the totalizer gate. When the totalizer gate is closed (stopping the input signals), an "inhibit" feedback signal prevents the display timer from being responsive to the

interim time base signals. Some time later (as determined by the DISPLAY TIME setting) the display timer automatically returns to its original state. In so doing, it trips the reset pulser which continues to hold the totalizer gate closed via the OR gate. In addition, the reset pulser causes the totalizer and two decade scalers with reset (Figure 4) to reset to zero. At a still later time (no greater than 0.1 second), a time base signal from the 10 cps decade scaler trips the reset pulser back to its original state. When the reset pulser returns to its original state, it removes the close gate signal to the totalizer gate and allows totalizing to begin again. The "inhibit" signal to the display timer disappears so that the next time base signal will toggle the timer and stop the totalizing (0.1, 1, or 10 seconds later) thus providing the gating period as selected by the Function Selector switch.

It is to be noted that the reset pulser is synchronized on 0.1 second pulses, thus assuring that the two decade scalers producing the 1 and 10 second time bases start at their own zero simultaneously with the start count signal.

3.2.3 Self-Test

When the F/R-P/T switch is in the P/T (PERIOD/TEST) position and the Function Selector switch is set to read FREQ B, all logic for frequency measurement is performed as described above; however, the input signal that is totalized is not signal B, but is a precise 10 kc signal derived from the internal 100 kc clock.

3.2.4 Time Base

The time base signal flow begins with the 100 kc oscillator. The signal is scaled down successively by four decade scalers to produce 10 kc, 1 kc, 100 cps, and 10 cps. The 10 cps signal (which is also the 0.1 second gate control) passes via the Function Selector switch to the two resettable decade scalers. These last two scalers (whose outputs are 1 cps and 0.1 cps) produce the corresponding 1 second and 10 second gate control signals.

3.3 PERIOD MEASUREMENT

3.3.1 Input Signal Flow

Only signals present at the signal A input amplifier can be measured for period. The A input signal is amplified, squared up and passed to the Function Selector switch. From here the signal is used to control the totalizer gate. Depending on the setting of the function selector (RATIO B/A for 1, 10 or 100 periods) the input signal may be divided down in frequency by 10 or 100 by decade scalers. This determines whether the totalizer gate will remain open for 1, 10 or 100 periods of the input signal.

The F/R-P/T switch must be in the PERIOD/TEST position. This applies precise internally generated 10 kc pulses to the totalizer gate.

THIS DRAWING CONTAINS INFORMATION DEEMED TO BE PROPRIETARY. THE FURNISHING OF THIS DRAWING DOES NOT CONFER ANY RIGHT IN OR LICENSE TO USE IT OR THE INFORMATION DISCLOSED HEREIN.

UNLESS OTHERWISE NOTED
1. NPN TRANSISTORS ARE ANADEX SPEC. #2404 OR EQUIV. PNP TRANSISTORS ARE ANADEX SPEC. #2405 OR EQUIV.
2. RESISTOR VALUES ARE IN OHMS ±10%, 1/4 W.
3. CAPACITOR VALUES ARE IN PICOFARADS.
4. DIODES ARE ANADEX SPEC. #2541 OR EQUIV.

Figure 4. Decade Scaler With Reset - Schematic Diagram

3.3.2 Counting and Logic

The totalizer counts 10 kc pulses during the time interval that the totalizer gate is open. The logic of the system, including gating, display and resetting is all identical with that described in paragraph 3.2 Frequency Measurement. The function of the input signal and the internal 10 kc signal are merely inetrchanged.

3.4 RATIO MEASUREMENT

3.4.1 Input Signal Flow

For ratio measurement both signals A and B are directed to the function selector switch following amplification and shaping. The operator adjusts the function selector switch so that the signal with the lowest frequency controls the totalizer gate and the higher frequency signal is counted by the totalizer while the gate is open.

As shown on the block diagram, the F/R-P/T switch must be in the FREQ/RATIO position to connect amplifier B to the function selector switch.

3.4.2 Counting and Logic

With the function selector switch in the A/B position, signal A is counted while signal B controls the totalizer gate. The reverse is true with the B/A function selected.

For greater accuracy the operator may choose to divide the gate-controlling frequency by 10 or 100. Therefore the gate will remain open for 10 or 100 periods as compared to 1 period. The totalizers will indicate the number of cycles of the higher frequency signal that occur during 1 (or 10 or 100) period (cycle) of the lower frequency. This is read as the ratio of the higher to the lower signal.

The logic of the totalizer and gating system is identical with that described in paragraph 3.2 Frequency Measurement.

SECTION IV

CIRCUIT DESCRIPTIONS

4.1 INPUT AMPLIFIER

Input amplifiers A and B are identical (see Figures 5, 6 and 7). Maximum sensitivity is 100 mv rms.

Q1 is a high gain amplifier with positive feedback via R6. Zener diode CR2 isolates Q1 from line voltage changes. CR1 clamps to ground the positive going output of Q1.

Q2, Q3 and Q4 further amplify the signal and square it off sharply (Q3 and Q4 are a Schmitt trigger). The output, taken from the collector of Q3, may be either a square wave or pulse, depending on the symmetry of the input signal.

4.2 DECADE COUNTERS

Nixie-type indicator tubes are active elements in five ring-type decade counters that form the totalizer section of the frequency/ratio counter. The characteristic block diagram of a decade counter is shown in Figure 8.

4.2.1 Block Diagram Discussion

Starting with the 0 toggle in the "on" condition (the Nixie 0 is "on" and all other toggles "off"), a negative pulse is applied to the input of the ring driver amplifier where it is inverted and amplified. The output of the ring driver amplifier is a positive pulse that starts at approximately +7 volts and rises to approximately +27 volts before returning to +7 volts, thus applying a positive pulse of about 20 volts to the ring pulse line. This ring turns off any "on" toggle without affecting the "off" toggles. Thus, toggle 0 is turned "off" by the first ring pulse. When toggle 0 turns "off", the carry line to toggle 1 changes from approximately +7 volts to about +50 volts, thus applying a positive pulse to the input of toggle 1. The ring pulse is of short duration compared with the carry pulse so that it has disappeared while the carry pulse is still effective to turn toggle 1 "on." Similar transfer of the "on" state is continued down the chain by successive ring pulses. When the carry pulse from toggle 9 to toggle 0 causes the latter to turn "on," a negative pulse is taken from the latter for use as the input signal to the ring driver amplifier of the next decade.

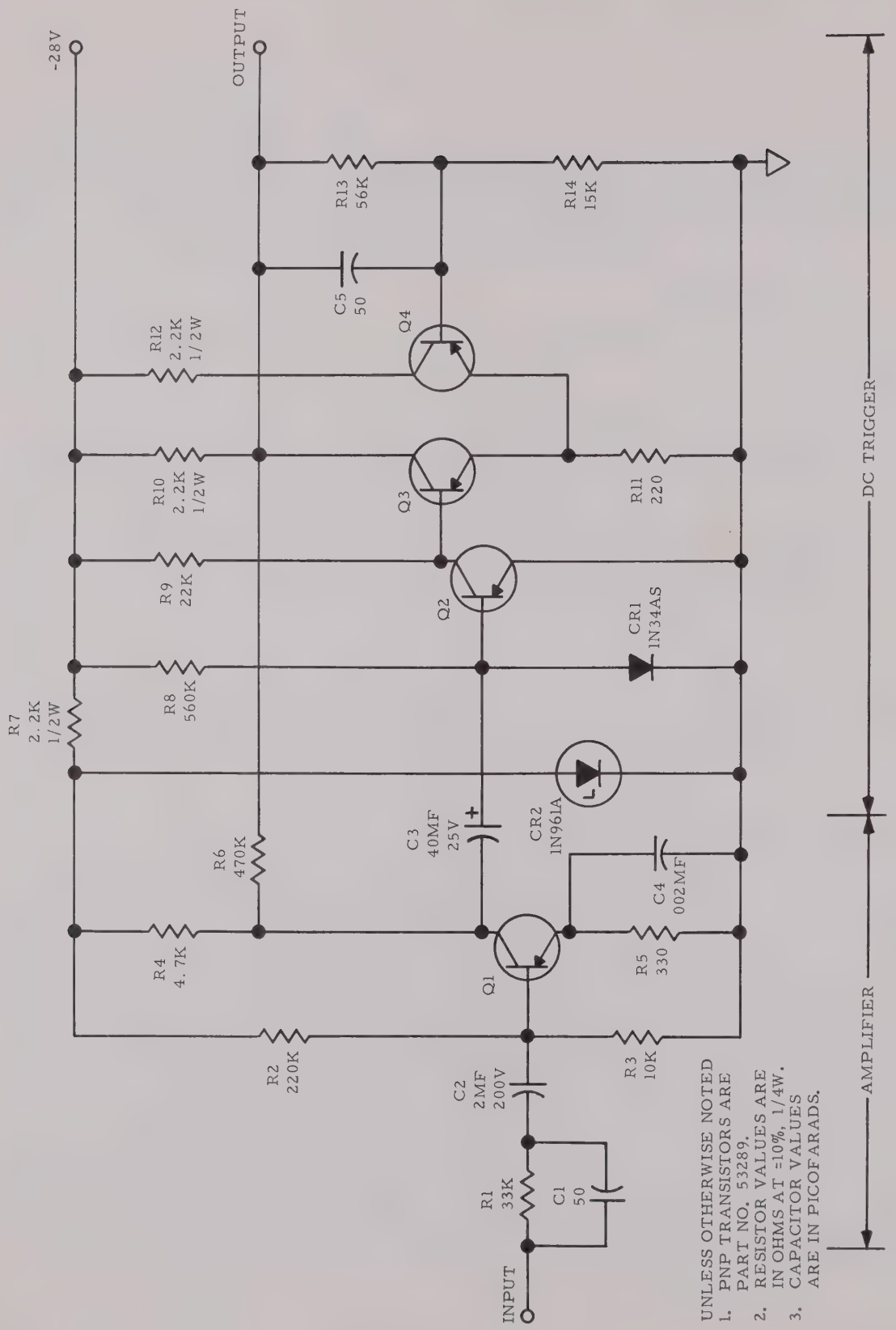


Figure 5. Input Amplifier Schematic Diagram

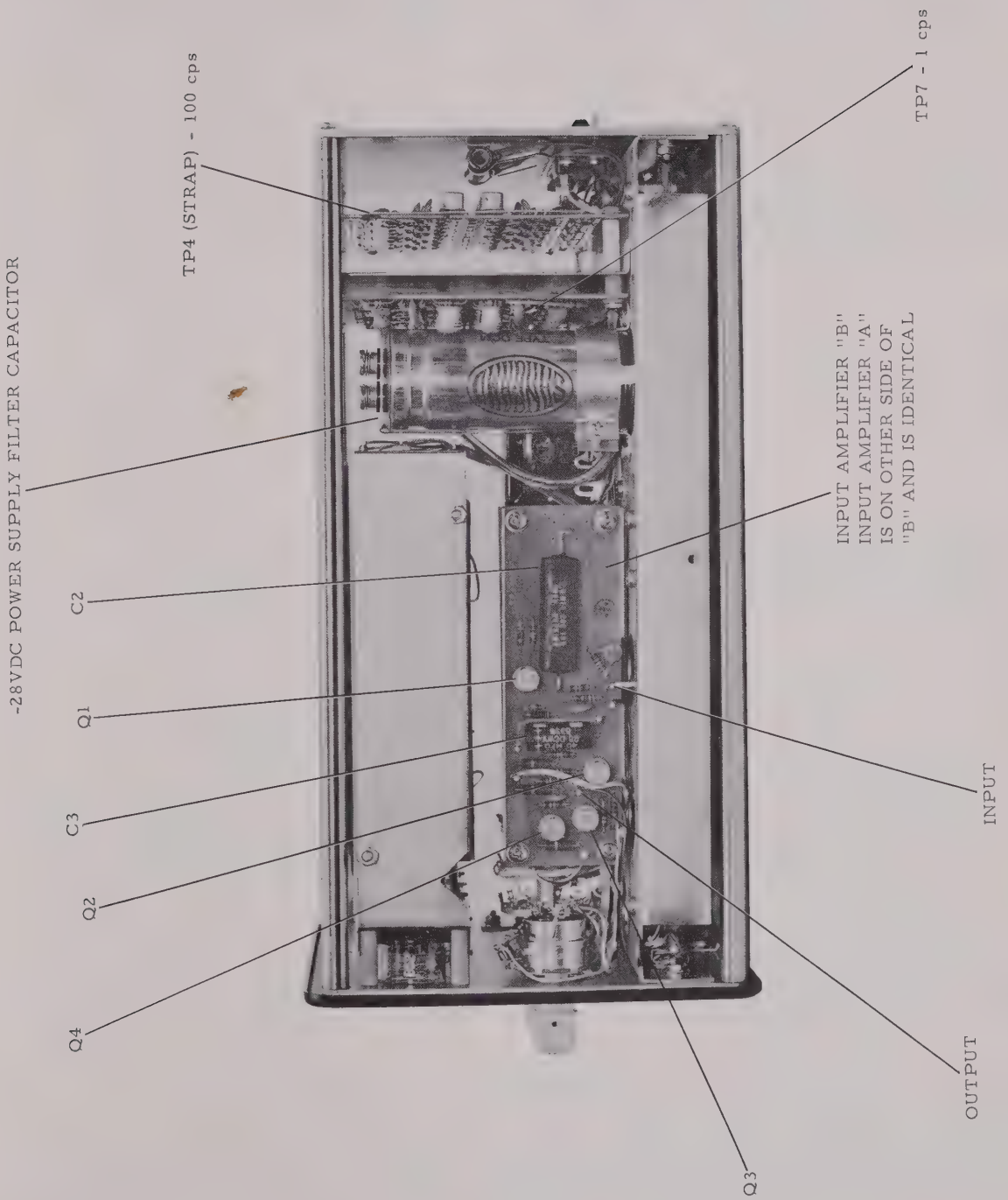


Figure 6. Right Side View - Frequency/Ratio Counter

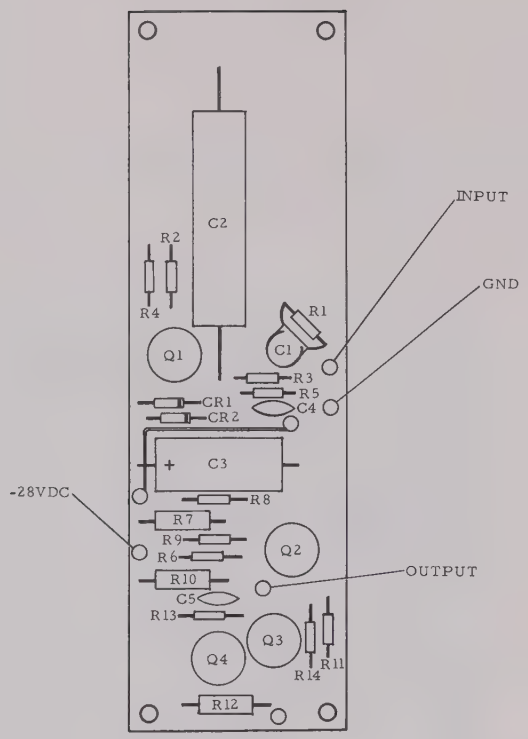


Figure 7. Component Locations For Input Amplifier

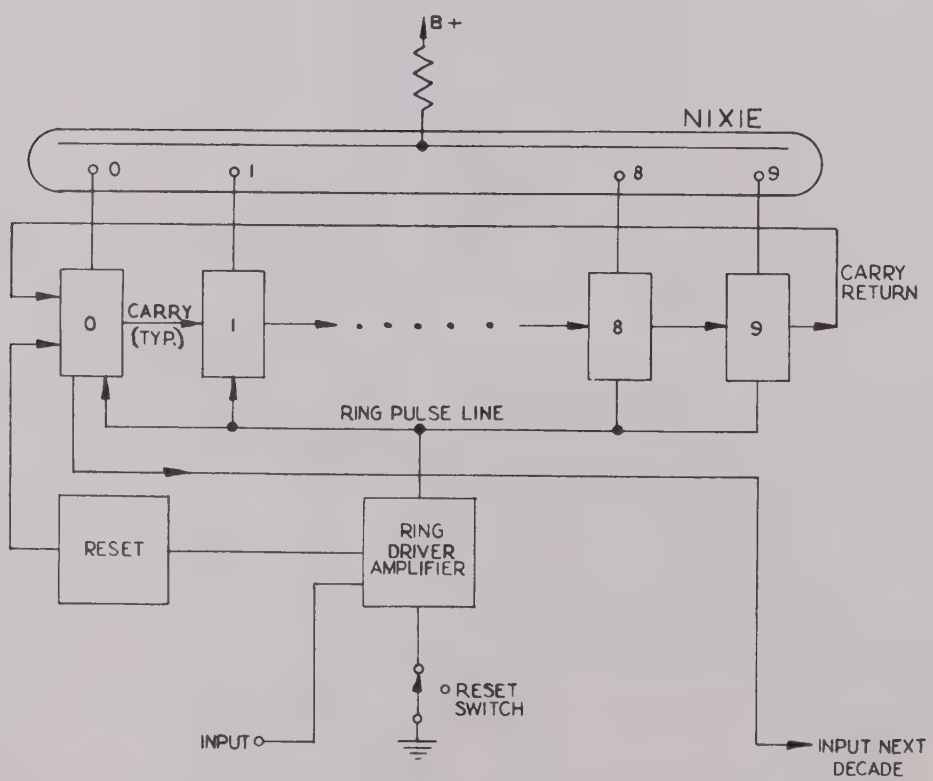


Figure 8. Decade Counter Block Diagram

The schematic of a typical toggle is shown in Figures 9 and 10. There are ten such toggles per decade. Also shown are the voltages to be expected at the various points for the "on" condition (Nixie numeral glowing) and the "off" condition (Nixie numeral not glowing). The voltages shown beneath vary with the line power and are approximate, i.e., +7v/+50v.

4.3 DISPLAY TIMER

The stop count signal couples to the display timer (Figure 11) through C5 and Q6 inhibit gate. At the end of the time delay interval, as determined by the setting of R18 and feedback capacitor C6, a positive pulse from the collector of Q7 is used to trip the reset pulser via C7.

4.4 RESET PULSER

As noted in paragraph 4.3, a pulse via C7 and CR7 trips the reset pulser. This flip-flop stays in this condition until reset via the start count pulse.

4.5 OR GATE

The two diodes (Figure 11) CR4 and CR5 form an OR gate with its output at the junction of voltage divider R27, R28, and speed-up capacitor C8. This point is near ground potential unless either of its two inputs are at -22 volts, which is the case if the display timer or reset pulser is in the trip condition.

4.6 TOTALIZER GATE

Whenever the OR gate output exists, i.e. -11 volts, saturation of Q1 (Figure 11) is assured. This results in Q3 also being saturated because of the bias to +235 volts through R7; therefore, the frequency-to-be-counted signal is shunted to ground and does not appear at the base of Q4.

When all inputs to the OR gate disappear, Q1 cuts off and permits the R1, R4 bias point to cause Q3 to cut off. The input signal is no longer shunted to ground, and its positive swing through CR1 causes the one-shot of Q4 and Q5 to emit sharp pulses that are entered into the totalizer.

4.7 100 KC OSCILLATOR

The 100 kc crystal controlled oscillator (Figure 12) is the source of precise frequencies and time intervals used in this instrument. The crystal X1 and transistors Q1 and Q2 generate a precise 100 kc signal which is amplified and squared by trigger Q3 and Q4 and power amplifier Q5.

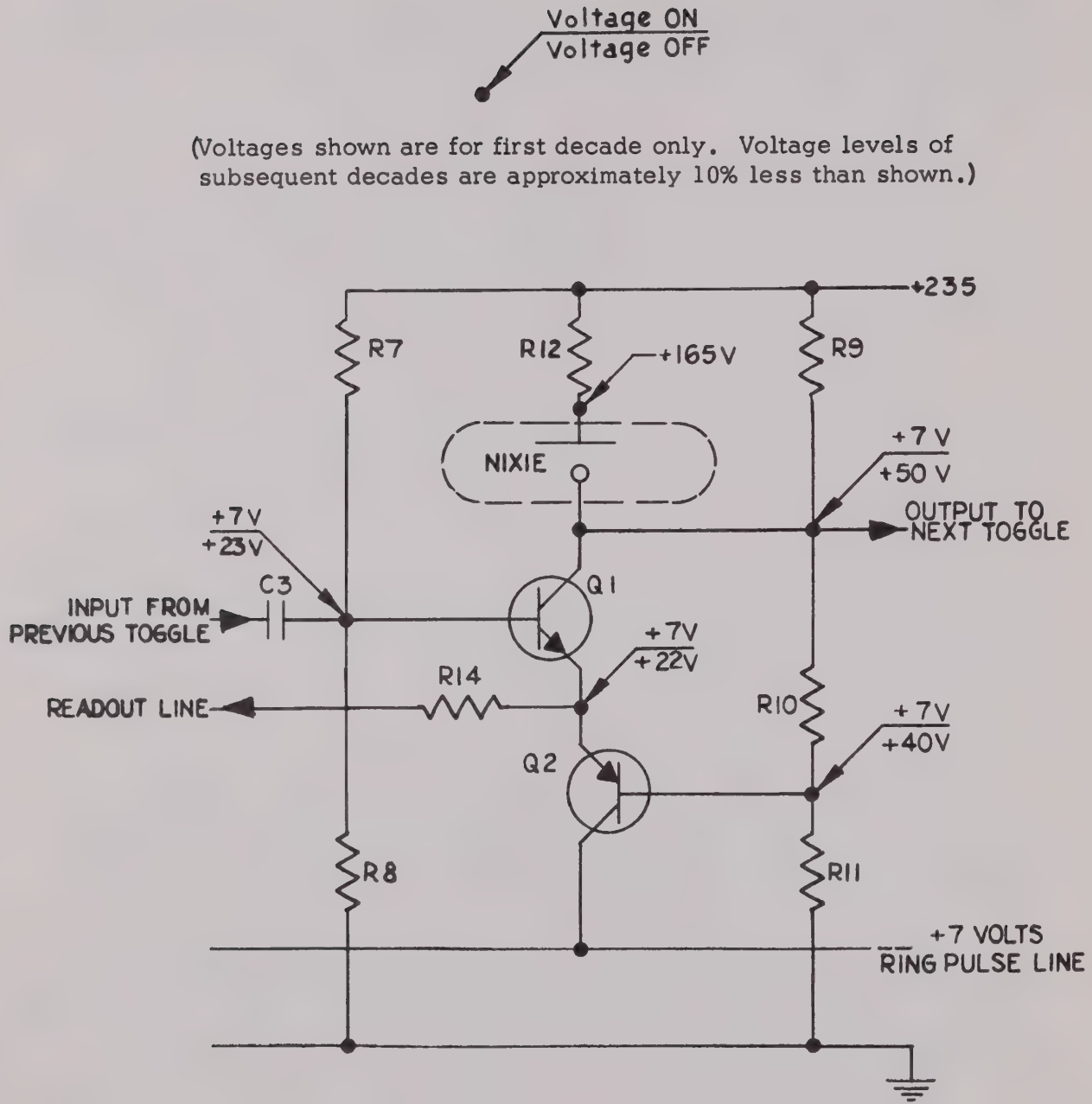


Figure 9. Toggle Schematic Diagram

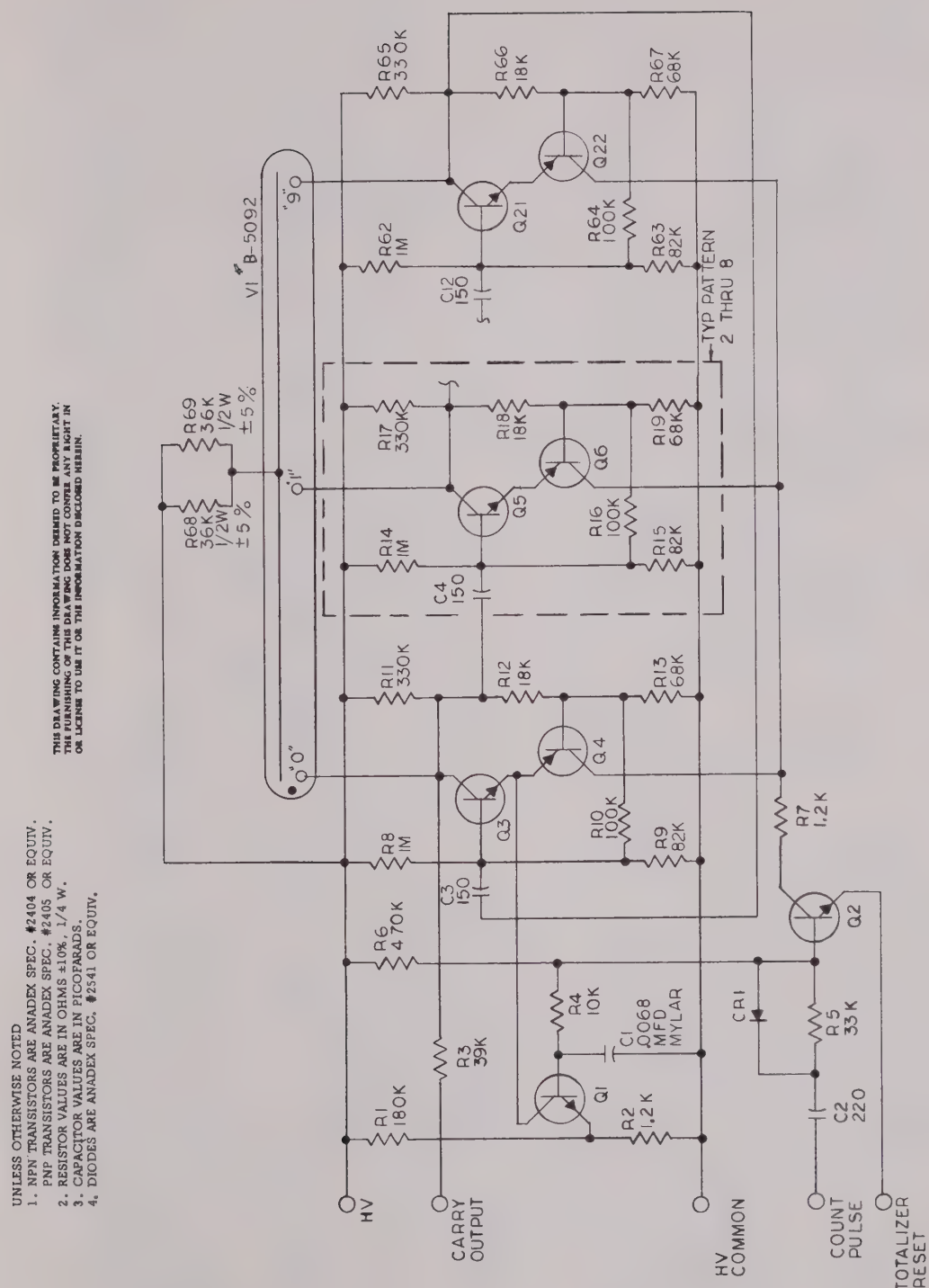


Figure 10. Decade Counter Schematic Diagram

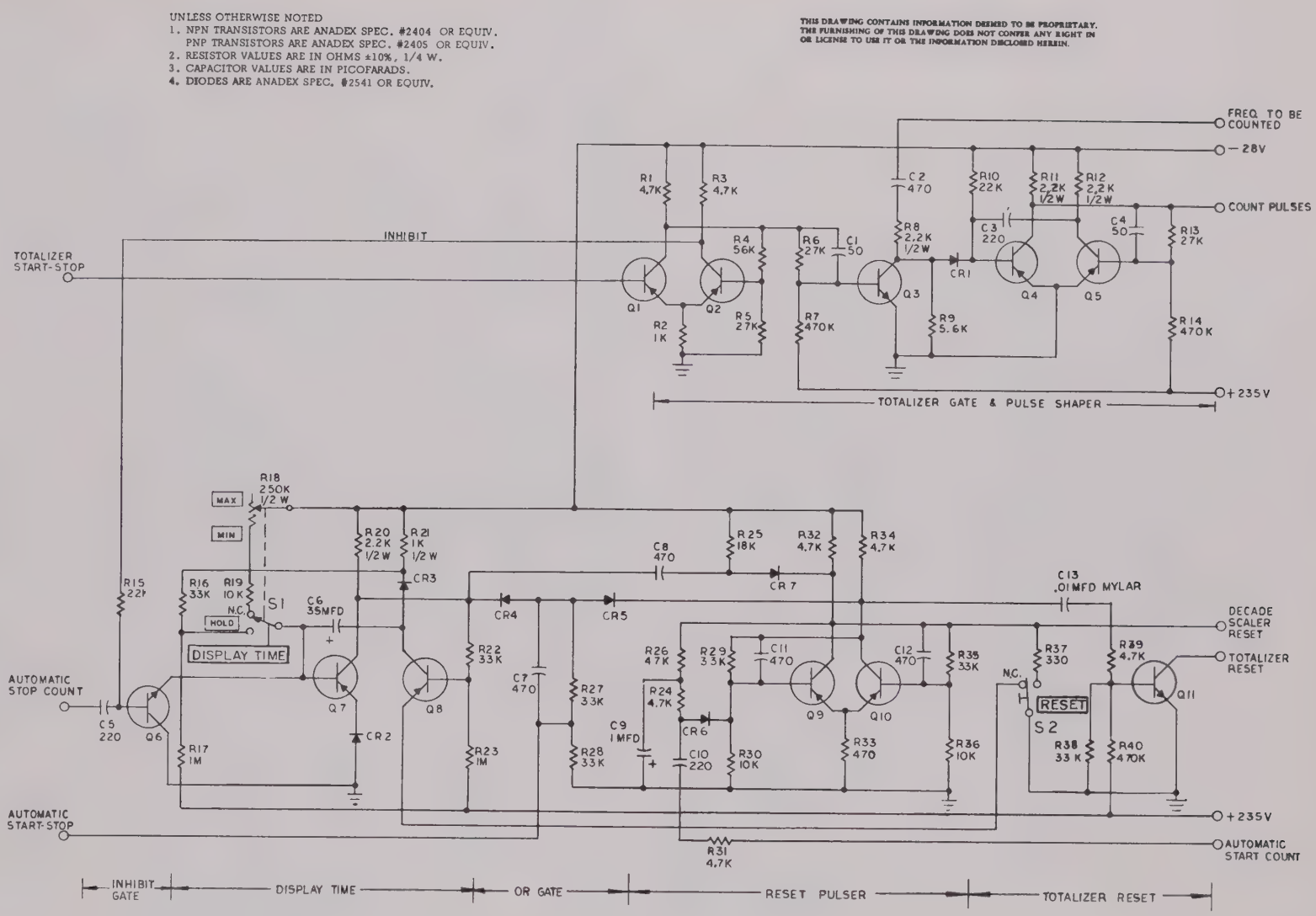


Figure 11. Control Logic Schematic Diagram

THIS DRAWING CONTAINS INFORMATION DEEMED TO BE PROPRIETARY. THE FURNISHING OF THIS DRAWING DOES NOT CONFER ANY RIGHT IN OR LICENSE TO USE IT OR THE INFORMATION DISCLOSED HEREIN.

UNLESS OTHERWISE NOTED

1. NPN TRANSISTORS ARE ANADEX SPEC. #2404 OR EQUIV.
   PNP TRANSISTORS ARE ANADEX SPEC. #2405 OR EQUIV.
2. RESISTOR VALUES ARE IN OHMS ±10%, 1/4 W.
3. CAPACITOR VALUES ARE IN PICOFARADS.

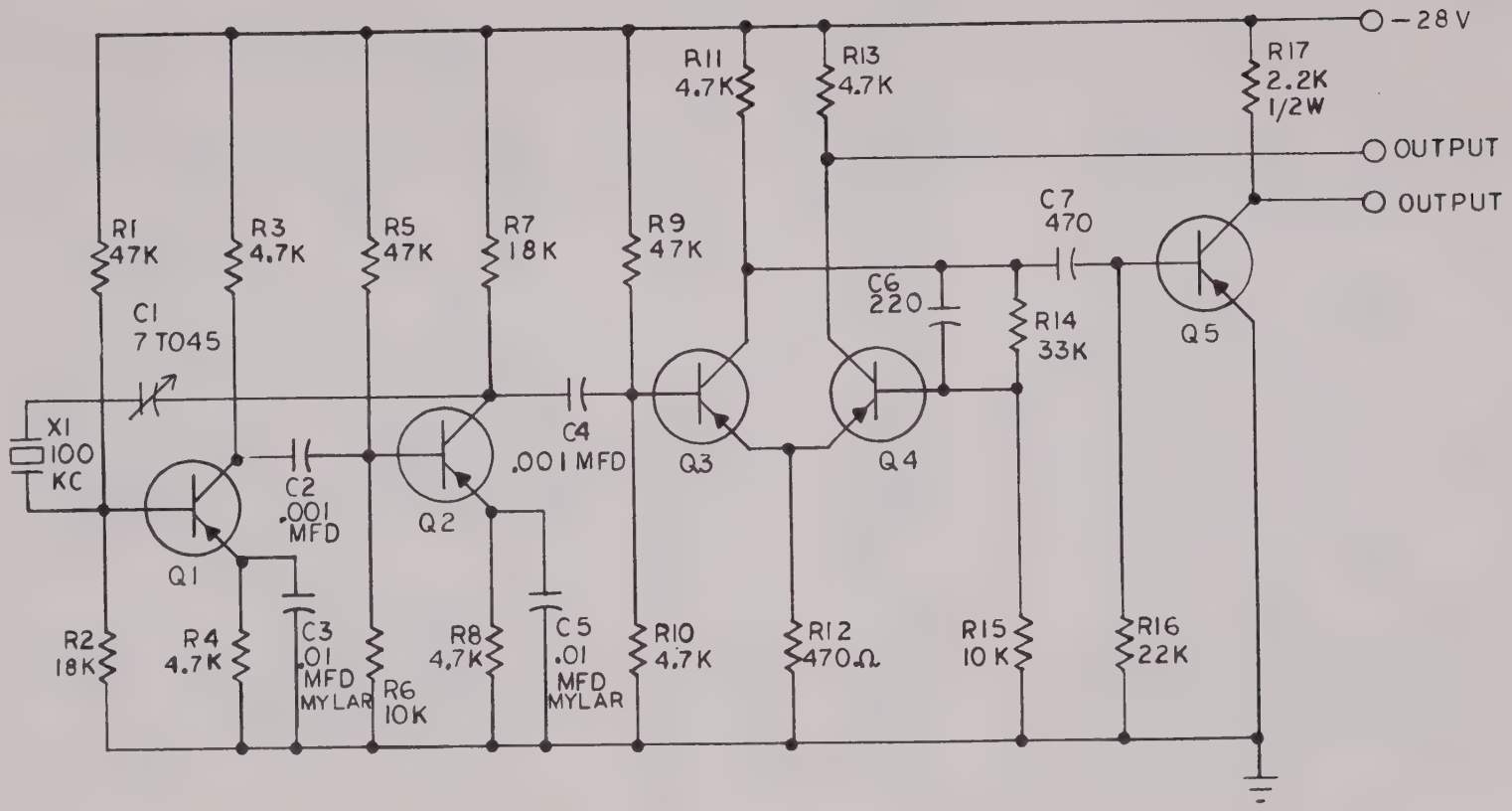


Figure 12. 100 kc Oscillator Schematic Diagram

4.8 DECADE SCALER

This decade scaler (Figures 4 and 14) consists of 4 binary counters with feedback to provide a scale of 10. The input signal is applied to the first binary Q1 and Q2 through capacitor C1. This binary drives the next binary through capacitor C4, and so on. The feedback circuit which changes the scale of 16 to a scale of 10 is transistor Q9 and diodes CR1 and CR4. This circuit provides a feedback pulse to the first and second binaries when the third binary switches to the "off" position. In this way, an output pulse is obtained for every 10 input pulses. Those decade scalers which must start their timing sequence from a zero condition must be reset before each timing interval. These decades (Figure 14) are reset by transistor Q10.

4.9 RESET

The output of the reset pulser (Figure 11) is used to reset the time base decades as well as the totalizer decades. The same thing is accomplished by the manual RESET push-button. This pushbutton, in addition, open circuits transistor Q8 so that a new cycle may be initiated when on hold.

4.10 POWER SUPPLY

The power supply (Figure 13)converts 105-125 vac line power to -28 vdc, +200 vdc, and +235 vdc for use in the Frequency/Ratio Counter module.

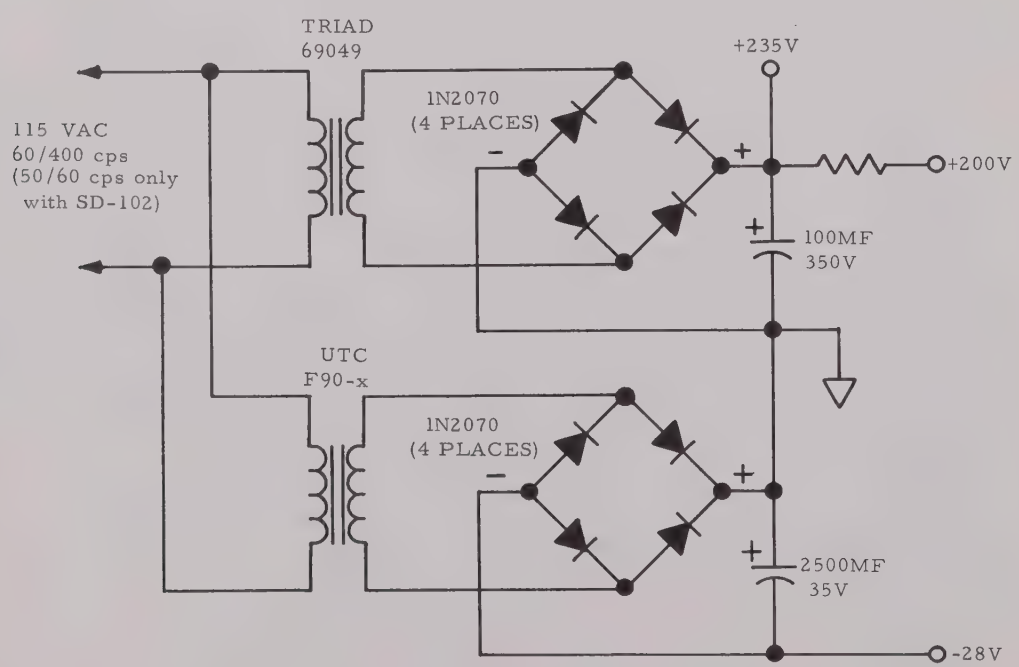


Figure 13. Power Supply Schematic Diagram

UNLESS OTHERWISE NOTED
1. NPN TRANSISTORS ARE ANADEX SPEC. #2404 OR EQUIV.
PNP TRANSISTORS ARE ANADEX SPEC. #2405 OR EQUIV.
2. RESISTOR VALUES ARE IN OHMS ±10%, 1/4 W.
3. CAPACITOR VALUES ARE IN PICOFARADS.
4. DIODES ARE ANADEX SPEC. #2541 OR EQUIV.
THIS DRAWING CONTAINS INFORMATION DEEMED TO BE PROPRIETARY. THE FURNISHING OF THIS DRAWING DOES NOT CONFER ANY RIGHT OR LICENSE TO USE IT OR THE INFORMATION DISCLOSED HEREIN.
INPUT
OUTPUT
-28V
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9

Figure 14. Decade Scaler Schematic Diagram

SECTION V

MAINTENANCE AND CALIBRATION

5.1 CALIBRATION OF 100 KC OSCILLATOR

This instrument contains only one adjustment. The 100 kc crystal oscillator, which has been factory adjusted before delivery, may require recalibration approximately every 12 months to compensate for crystal aging. The adjustment is a trimmer capacitor C1 (Figures 15, 16, and 17) and is located adjacent to the crystal. The 100 kc signal is available at test point 1, Figure 12.

NOTE

This test point is the collector of Q5, the oscillator output amplifier. The signal is a 20 v p-p square wave.

5.2 ROUTINE MAINTENANCE

Using a low pressure (less than 50 psi) dry air source, blow the dust out of the unit occasionally. Particular attention should be paid to the totalizer section where excessive dust could cause leakage paths for the +235 volt Nixie drive voltage.

5.3 MALFUNCTION AND REPAIR

This counter uses straight forward digital-type circuitry throughout. By consulting the theory of operation section, the unit block diagram and the photographs showing key test points and components, the technician should be able to quickly locate the defective circuit. A high quality dc-coupled dual beam oscilloscope (example: Tektronix Type 502) will prove most helpful in this effort.

All circuits except the input amplifiers may be checked with the F/R-P/T switch in the PERIOD/TEST position and the function selector in FREQ B, with time base of 0.1 second.

External signals must be applied to the input amplifiers to check their performance. With a 100 mv rms input signal, amplifier output should be approximately 20 v p-p.

5.3.1 Recommended Spares

Trouble shooting individual totalizer decade counters can sometimes be quite difficult in the field. To keep equipment down-time at a minimum it is recommended that the user stock a spare decade counter assembly (or better - a complete totalizer assembly).

Complete spare stock would also include (but not be limited to) a decade scaler board (Figure 15) a control logic board (Figures 16 and 17), and a decade scaler board with reset (Figures 18 and 19). Component locations for the decade counter are shown in Figures 20 and 21.

Replacement parts and assemblies are stocked by Spectral Dynamics Corporation. When ordering, please state the serial number of counter, the assembly or circuit affected, and a complete description of part including the circuit reference designation if known.

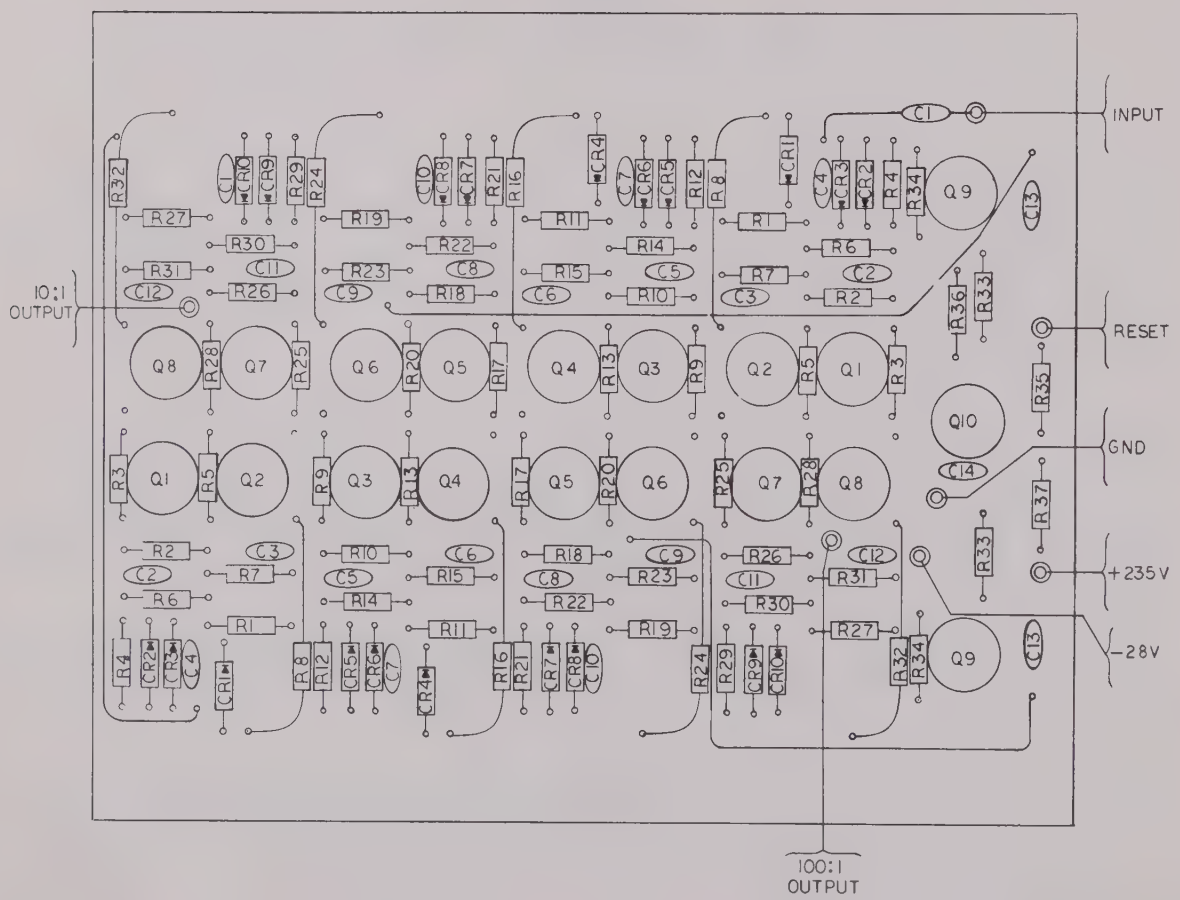


Figure 15. Component Locations For Decade Scaler

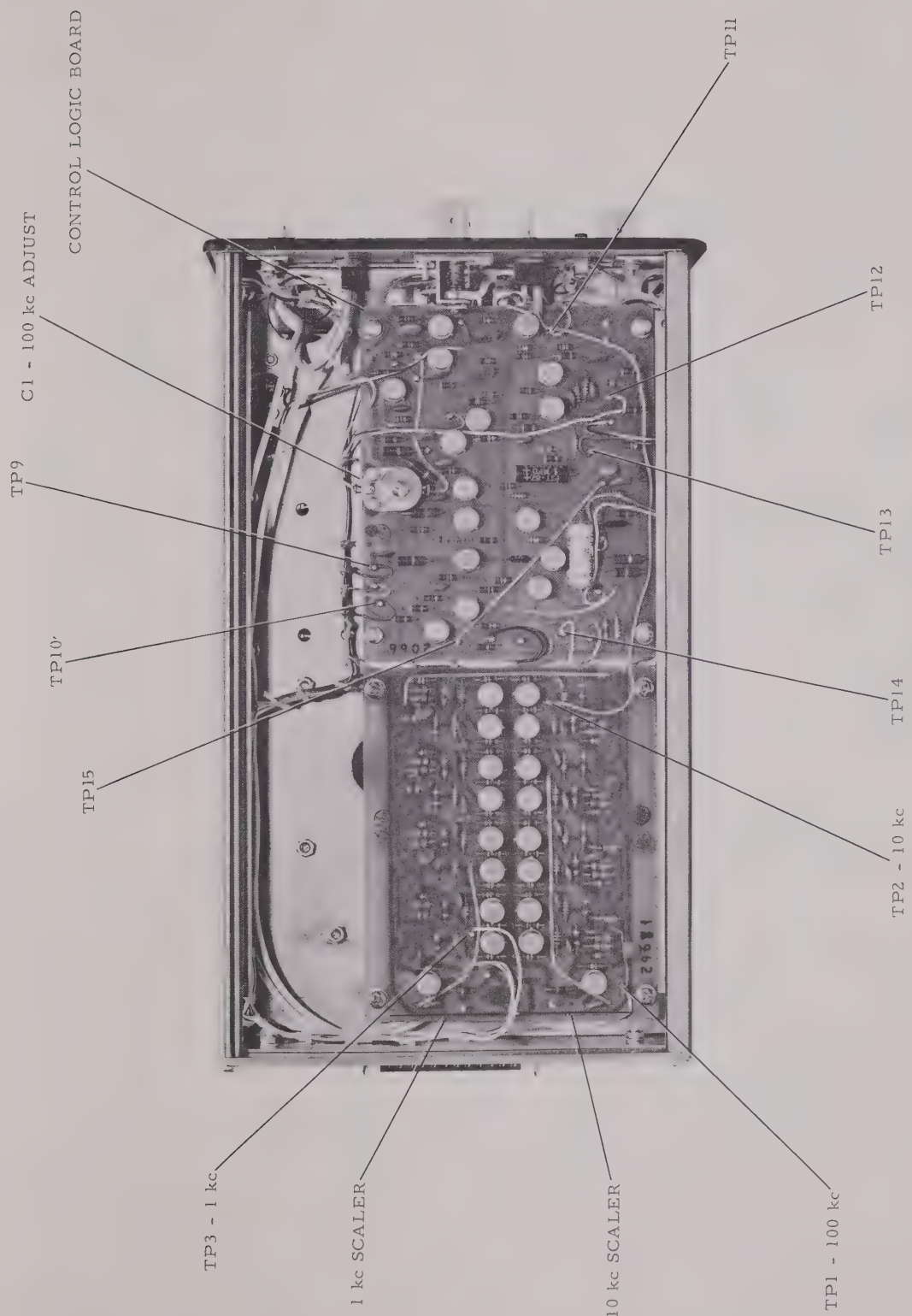


Figure 16. Bottom View - Frequency/Ratio Counter

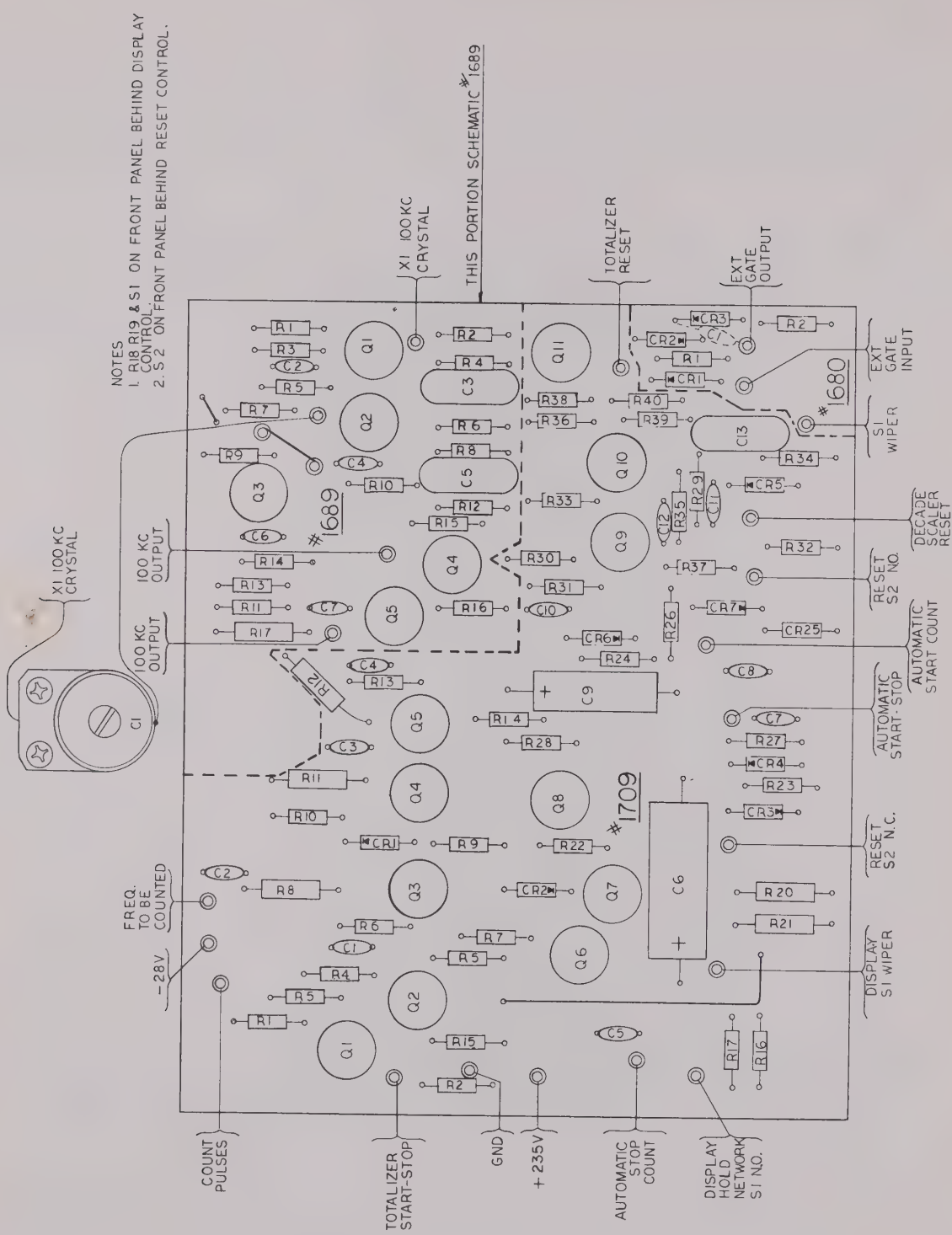


Figure 17. Component Locations For 100 kc Oscillator and Control Logic

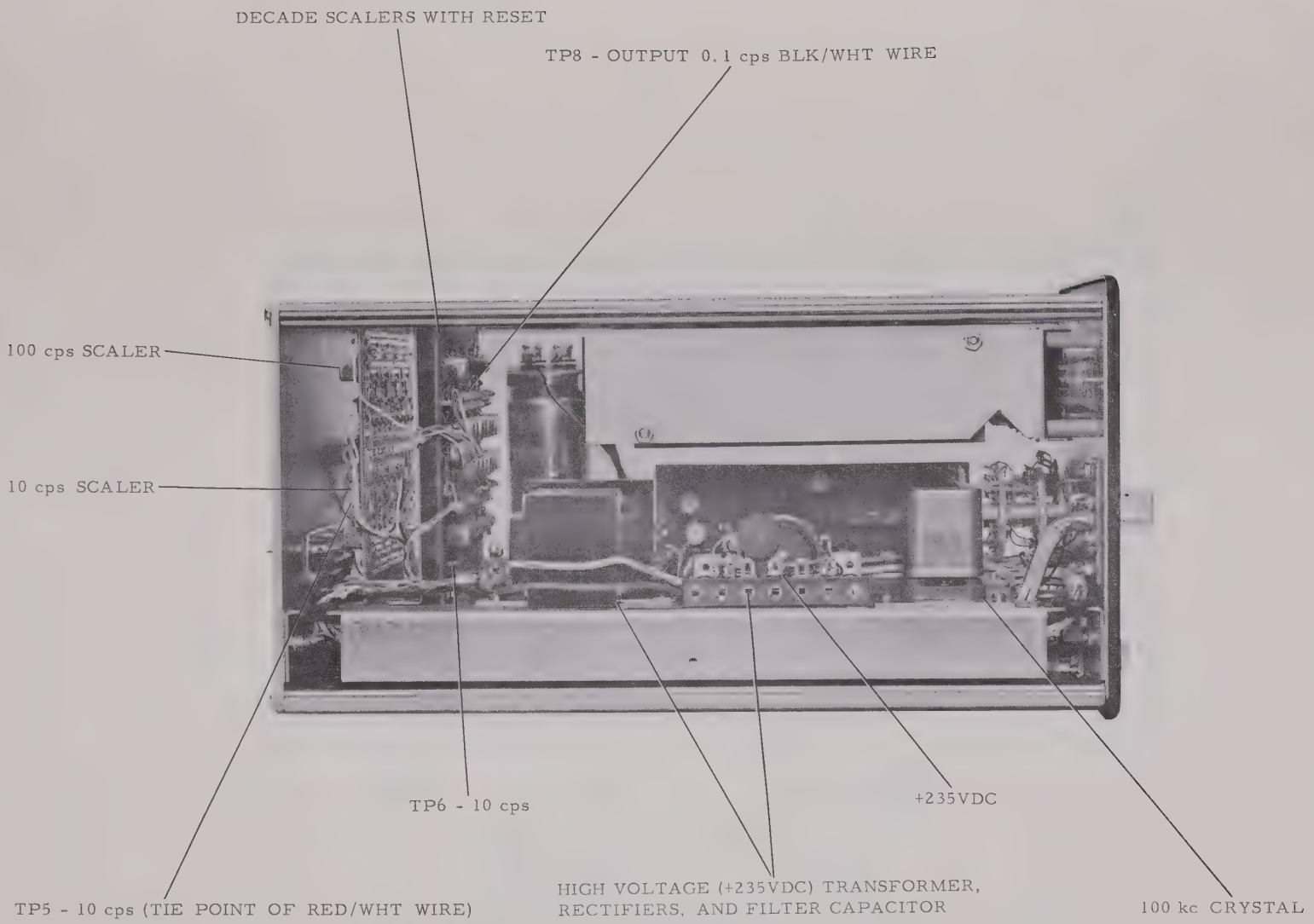

DECADE SCALERS WITH RESET
TP8 - OUTPUT 0.1 cps BLK/WHT WIRE
100 cps SCALER
10 cps SCALER
TP6 - 10 cps
+235VDC
TP5 - 10 cps (TIE POINT OF RED/WHT WIRE)
HIGH VOLTAGE (+235VDC) TRANSFORMER, RECTIFIERS, AND FILTER CAPACITOR
100 kc CRYSTAL

Figure 18. Left Side View Ratio Counter

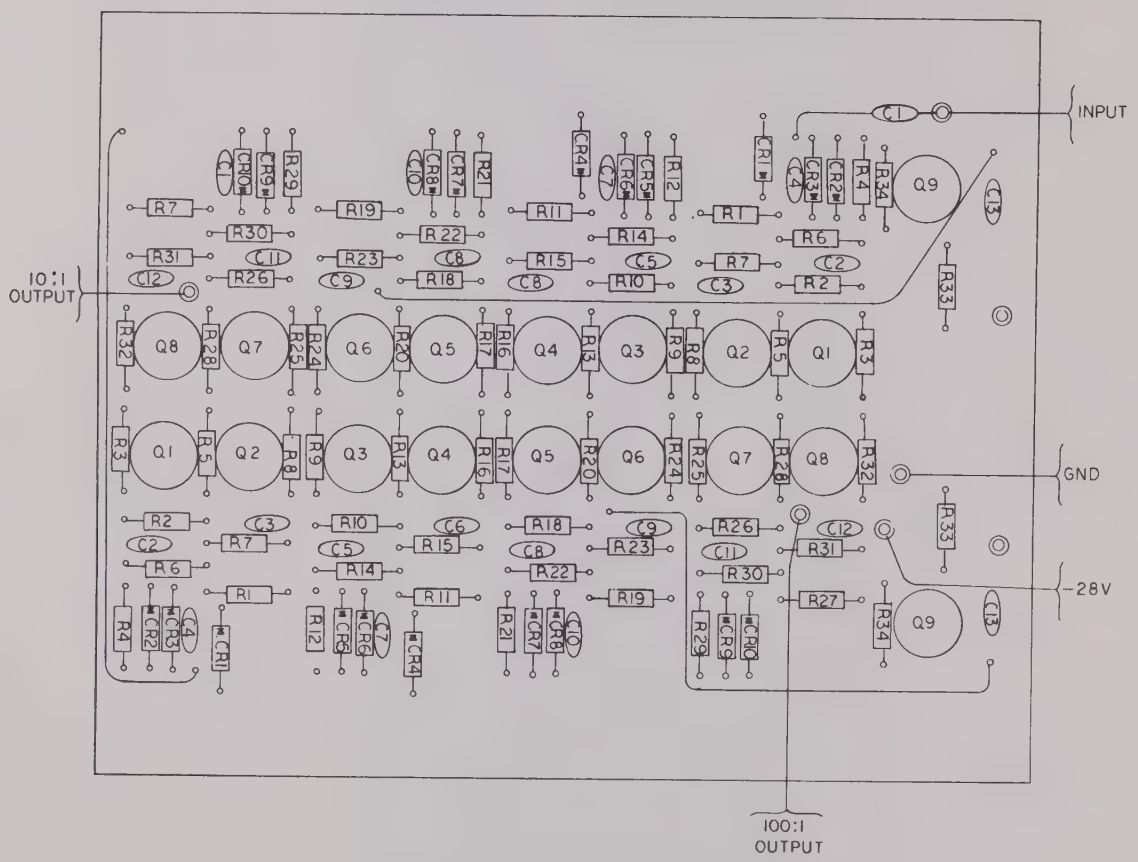


Figure 19. Component Locations For Decade Scaler With Reset

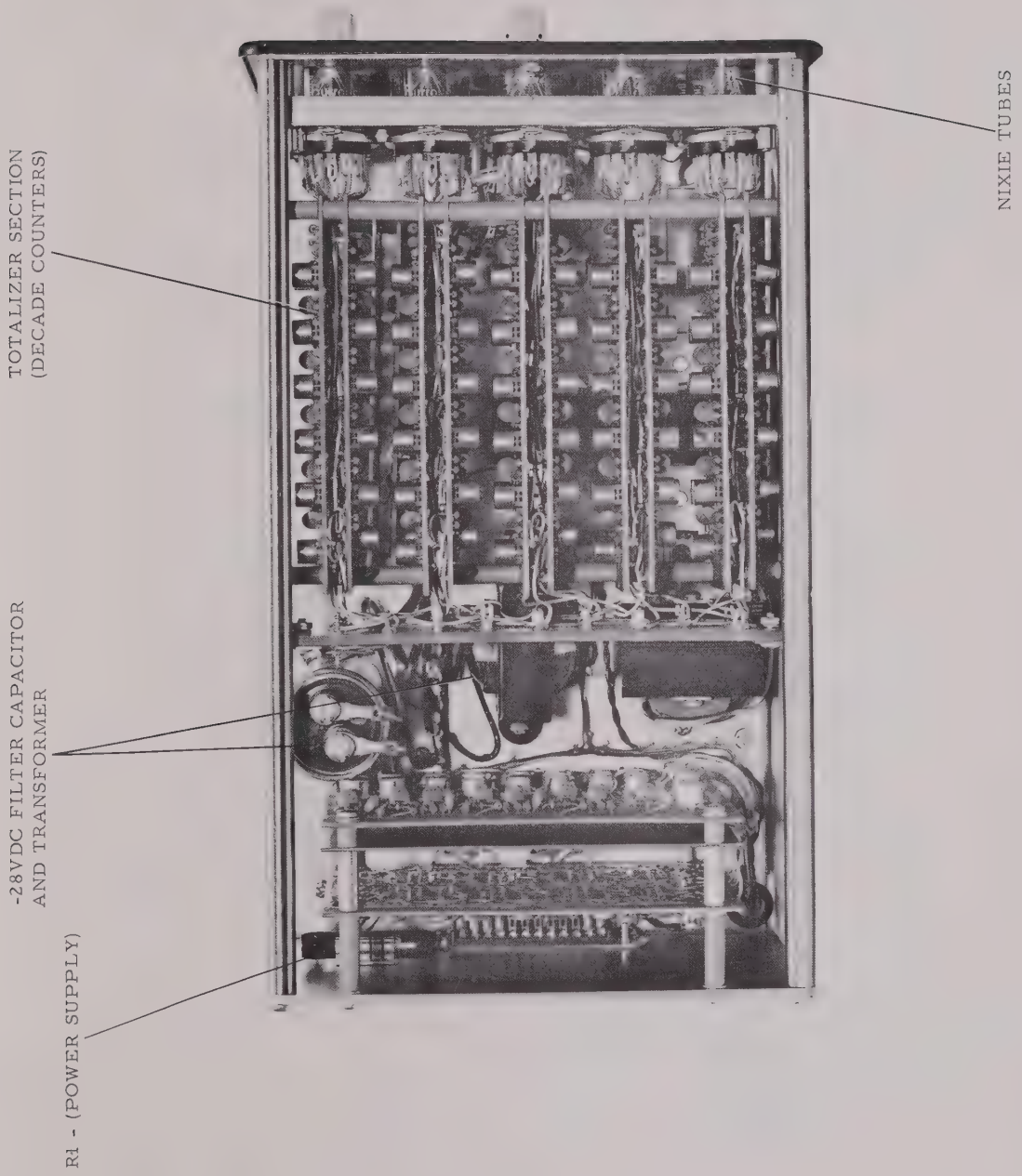


Figure 20. Top View - Frequency/Ratio Counter

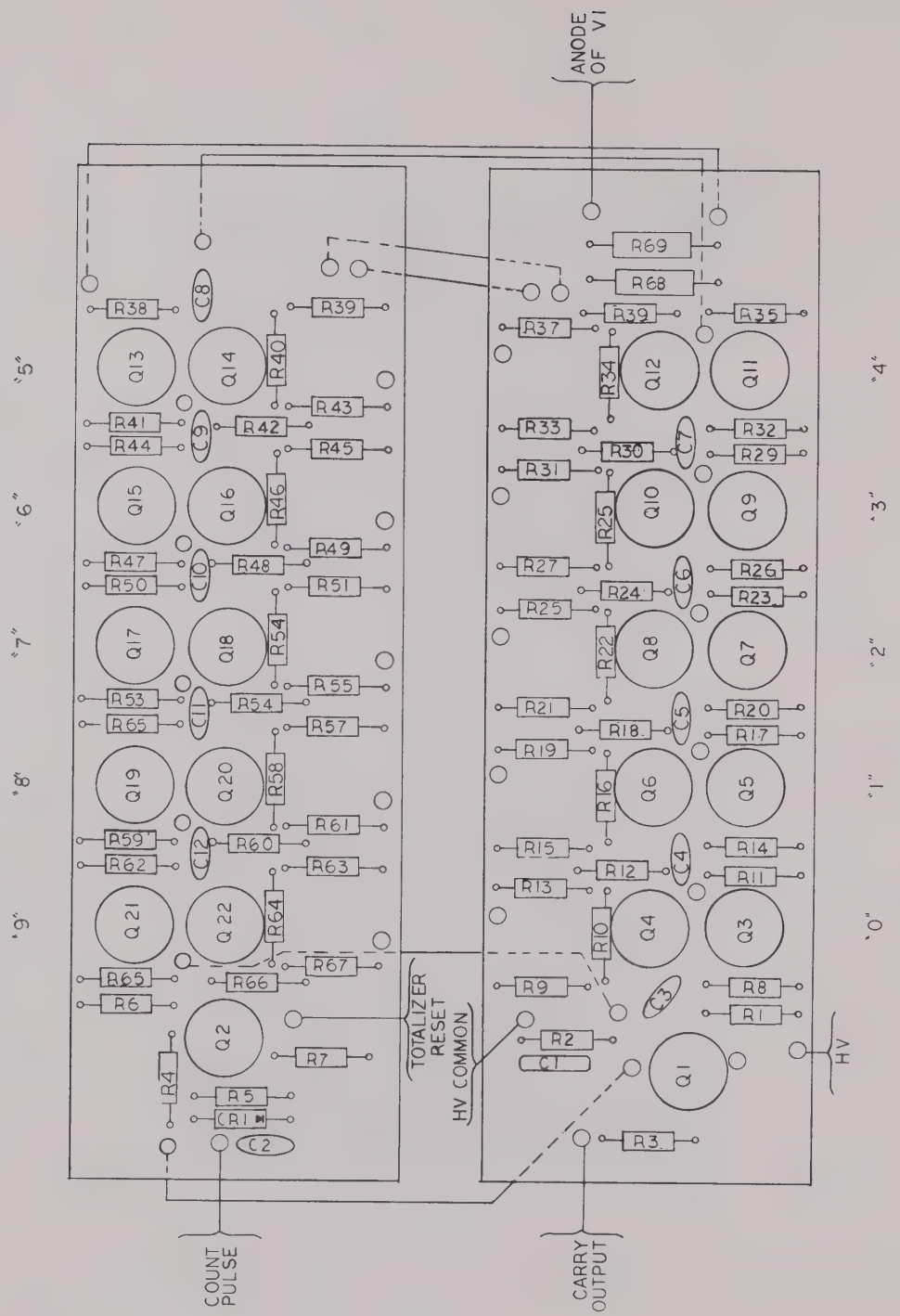


Figure 21. Component Locations For Decade Counter

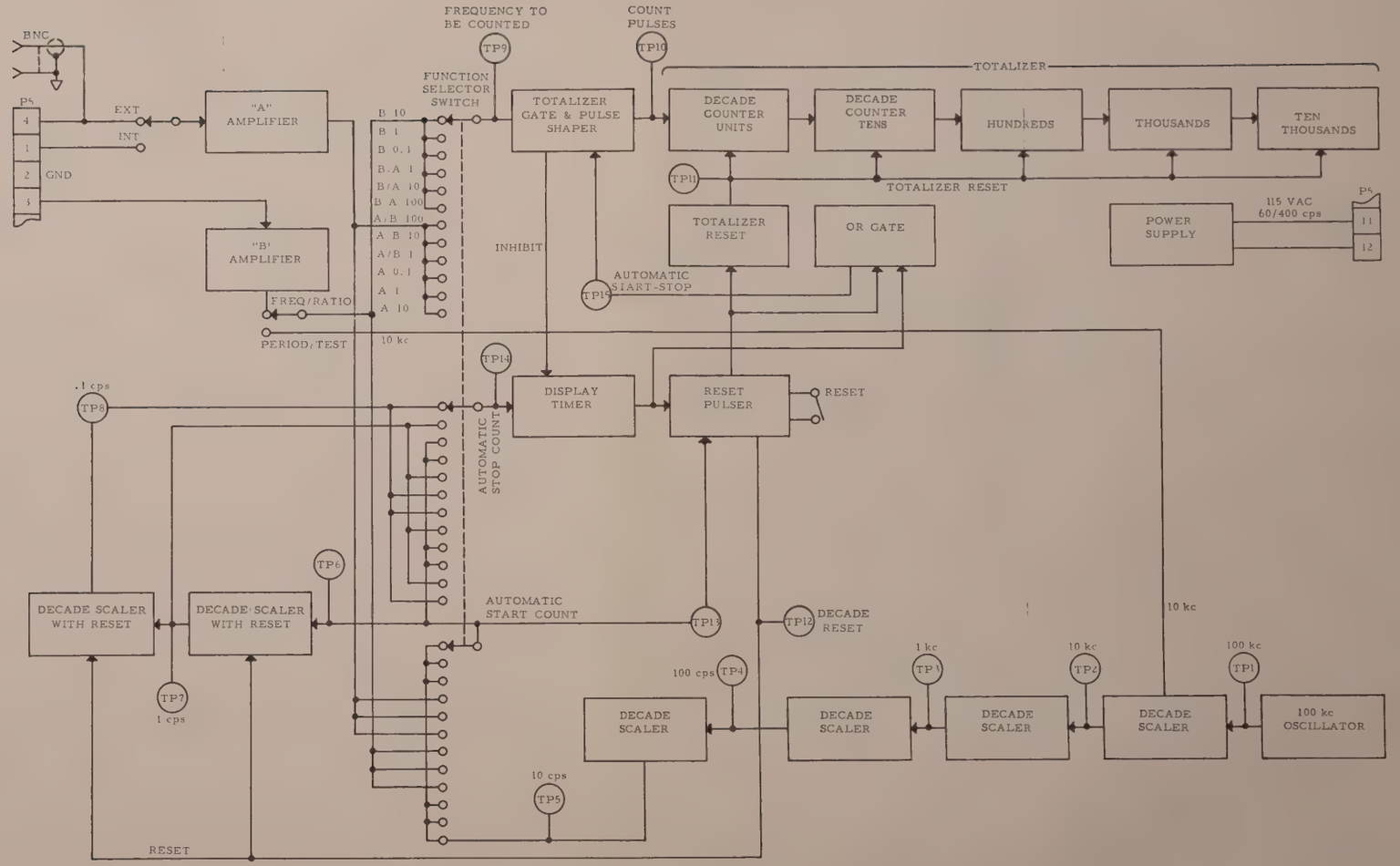


Figure 22. Frequency/Ratio Counter Block Diagram

SERIAL NUMBER _____

SCHEMATIC CHANGE LTR ____

INSTRUCTION MANUAL

SD102-10

GENERAL PURPOSE

TRACKING FREQUENCY MULTIPLIER

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

P. O. Box 671 8911 Balboa Avenue
San Diego, California
Telephone: (714) 278-2501

1 December 1964

TABLE OF CONTENTS

		Page
I.	Introduction	1
II.	Specifications	1
III.	Theory of Operation	2
IV.	Operating Procedure	3
V.	Calibration Procedure	5

LIST OF ILLUSTRATIONS

1. Figure 1 - Location of Test Points & Adjustments 8
2. Detailed Block Diagram, DWG. NO. 22127 Rear
3. Schematic, DWG. NO. 22104 Rear

GENERAL INFORMATION

I. Introduction.

The Model SD102-10 General Purpose Tracking Frequency Multiplier has been designed and built for use with the Spectral Dynamics Model SD102 Dynamic Analyzer Tuner (DAT). It will automatically track practically any type of repetitive wave form in the range of 10 cps to 12.5 kc and provide a tuning signal for the Model SD101A Dynamic Analyzer.

II. Specifications.

Input Frequency Range:	Selectable for any decade range: Sine: 10 cps to 12.5 kc Pulse: 20 cps to 12.5 kc
Input Wave Form:	Practically any repetitive signal. (sine wave, square wave, pulse, etc.)
Sensitivity:	50 mv rms to 65 volts rms, without adjustment.
Input Impedance:	10k ohm or greater.
Output Frequency Range:	TFM Mode: 1 cps to 30 kc (nominal) OSC Mode: 10 cps to 30 kc (nominal)
Output Wave Form & Amplitude:	Sine Wave ..... 3v p-p DC prop. to freq..... ±9v full scale Triangle Wave.....5v p-p Square Wave..... 5v p-p Conditioned Input..... 5v p-p
Output Impedance:	Less than 1k ohm for sine, square and triangle wave outputs. 10k ohm for dc output.
Multiplying or Ratio Range:	0.1 to 150 (nominal), depending on input frequency.
Accuracy:	Plus or minus 0.5%, static
Maximum Tracking Rate:	Sine: 10 cps to 500 cps - 20 sec/decade 500 cps to 12.5 kc - 7 sec/decade Pulse: 20 cps to 2.5 kc - 20 sec/decade 2.5 kc to 12.5 kc - 7 sec/decade
DC Output Linearity:	Plus or minus 0.25%

III. Theory of Operation. (Refer to detailed block diagram)

3.1 The TFM input signal (J12, SD102 main chassis, rear) is conditioned into a square wave and passed to the SD-102 main chassis. (The frequency of pulse input signals is divided by two during the conditioning process).

3.2 In the SD102 the conditioned input signal is converted to a pulse of constant width.

3.3 The constant width pulse is returned to the SD102-10 plug-in unit where it triggers a voltage controlled monostable. This monostable produces a pulse whose width is determined by the value of the monostable timing capacitor (UPPER INPUT FREQ (A) switch) and a variable biasing voltage (VERNIER control).

3.4 The resulting pulse energy is integrated by one of two low pass filters, producing a dc signal proportional to the input frequency, changing linearly with any change in input frequency. The dc signal is passed through normalizing and offset circuitry and then to the SD102 main chassis where it is converted back to an ac signal of desired frequency (see SD102 Theory of Operation).

3.5 Selection of low pass filters in step 4 is determined by settings of the UPPER INPUT FREQ (A) and PULSE/SINE switches. The low pass filter characteristics relate directly to the tracking-rate capability of the SD102-10 plug-in unit.

3.6 A self-contained voltage controlled oscillator (VCO) provides a test and calibration signal for the plug-in unit when in the PRESET mode. During routine operational set-up, the frequency of the VCO is set by the VERNIER control to coincide with the upper input frequency to be applied to the plug-in unit. This action automatically applies the correct bias to the voltage controlled monostable, assuring linear operation from the upper input frequency to a frequency one decade (factor of 10) lower.

3.7 In the OSC mode a fixed dc voltage is substituted for the normal dc proportional to input frequency. The SD102 and the SD102-10 combination then becomes a manually tuned oscillator, the output frequency being determined by the OUTPUT FREQ RANGE (B) controls.

IV. Operating Procedure.

To operate in TFM Mode:

1. Select PULSE or SINE input signal mode, depending on characteristics of input signal.

   NOTE: See SD102 Manual, page 14, for description of permissable input wave forms. Signal amplitude and frequency range must agree with specifications given on page 1 of this TFM manual.

2. Turn SD102 power switch to ON.

3. Place PRESET - OPERATE switch in PRESET.

4. Set the UPPER INPUT FREQUENCY (A) switch to a range position covering the highest input frequency to be applied to the plug-in during the course of this operation or test run.

5. Place frequency/ratio counter in FREQ A mode (See para. 2.4 of SD102 Manual for detailed counter operating procedures).

6. Adjust VERNIER control until counter reads upper input frequency. (See step 4 above)

7. Estimate what the output frequency (signal B) will be when the upper input frequency is multiplied by the desired ratio. Set the OUTPUT FREQUENCY RANGE (B) control to the appropriate range.

8. Place counter in FREQ B mode. , Adjust output frequency range (B) vernier control (small concentric knob) to display approximate output frequency on counter.

9. Place counter in RATIO B/A or A/B mode (See note below) and adjust output frequency range (B) vernier control for exact ratio desired.

   NOTE: If signal B is higher in frequency than signal A, read the frequency ratio in the RATIO B/A mode. Use RATIO A/B if the reverse is true. Readings obtained in RATIO A/B will be the reciprocal of the ratio of B to A (output signal to input signal).

10. Move PRESET - OPERATE switch to OPERATE. Apply TFM input signal to SD102 rear connector J12. The unit is now ready for operation. Signal B will track signal A, maintaining the preset ratio, while signal A is varied over a one decade range below the upper input frequency determined in step 4 above.

    If during any of the preceding instructions the output signal should disappear, momentarily move the SD102 power switch to RESET, then back to ON.

Notes on the use of the TRIGGERING controls:

a. In SINE mode operation the unit is automatically switched to AC coupling and AUTO triggering.

b. In the PULSE mode several alternate triggering methods are available. Most pulse applications are met with AC coupling and AUTO level control (triggering at the positive-going zero axis crossing).

c. For special pulse waveforms and test conditions, more reliable triggering may be obtained by using DC coupling and/or the variable LEVEL control. The LEVEL control allows triggering on the positive going input waveform at any point within plus or minus 1 volt of ground level.

Notes on the selection of the UPPER INPUT FREQ (A) range:

a. To give the fastest input signal tracking capability, the user should select the highest possible UPPER INPUT FREQ (A) range at all times.

b. At first glace it would appear that range selection is quite obvious and definite, since there is no apparent range overlap. However, this is not always true.

c. Consider the following example: The predetermined upper input frequency (A) is 490 cps. The total input signal frequency variation will be 400 cps (90 cps to 490 cps).

The user would normally select the 100 - 500 cps UPPER INPUT FREQ (A) range for this application, since 490 cps falls with this range. However, the 500 cps - 2.5 kc range is also usable for this application, and will provide a significantly faster tracking rate. As stated earlier, the input signal may be varied over a one decade range below the upper input frequency. One decade down from 500 cps is 50 cps. As long as the total input signal excursion falls within this range of 50-500 cps, the 500 cps - 2.5 kc UPPER FREQ INPUT (A) range may be utilized. Our example meets this requirement since the input signal will range between 90 and 490 cps.

d. If a particular application requires the fastest possible tracking rate, and if the total input signal excursion is less than one decade and falls near the upper end of a UPPER INPUT FREQ (A) range, the user should attempt to use the techniques outlined above to optimize the performance of the plug-in unit.

To operate as a manually tunable oscillator:

1. Place TFM - OSC switch in OSC.

2. Place counter in FREQ B mode.

3. Adjust the output frequency (signal B) over the range of 10 cps to 30kc, using the OUTPUT FREQUENCY RANGE (B) switch and vernier controls.

NOTE: In the OSC mode, a dc voltage proportional to output frequency is not provided at rear chassis connector J17.

CALIBRATION PROCEDURE FOR SD102-10 GENERAL PURPOSE TRACKING FREQUENCY MULTIPLIER

Equipment required: Laboratory grade dc coupled oscilloscope.
Audio Signal Generator.

> NOTE
>
> Refer to Figure 1 for location of test points & adjustments

1. Set Frequency/Ratio Counter to read FREQ. B.

2. Place UPPER INPUT FREQ (A) selector in the 500 cps - 2.5 kc position.

3. Place SINE/PULSE switch in PULSE position.

4. Place PRESET/OPERATE switch in preset position.

5. Place TFM/OSC switch in TFM position.

6. Place OUTPUT FREQUENCY RANGE (B) switch in the 300 cps - 1 kc position.

7. Operate the OUTPUT FREQUENCY RANGE (B) vernier control over its full range, checking to see that full coverage is provided. Adjust FULL SCALE potentiometer (R14) for approximately equal overlap on each end.

8. Place the PRESET/OPERATE switch in the OPERATE position.

9. Remove TFM input signal from J12 of SD102 (rear panel).

10. Short together terminals E1 and E2 on Card A13 using a single alligator clip or short jumper lead.

11. Measure the dc voltage at Test Point J1-6 using a digital voltmeter, high gain dc-coupled oscilloscope, or equivalent instrument. Adjust the OFFSET potentiometer (R10) for zero volts dc, plus or minus 1 millivolt.

12. Place SINE/PULSE switch in SINE position.

13. Adjust NORMALIZE potentiometer (R7) for zero volts at J1-6.

14. Remove short previously inserted between E1 and E2. Place PRESET/OPERATE switch in PRESET.

15. Place SINE/PULSE switch in PULSE position. Repeat step 6, checking for overlap on each end of the frequency range. (Note: If it is necessary to adjust FULL SCALE potentiometer (R14) for adequate overlap, steps 7 thru 14 must be repeated).

16. Remove short between E1 and E2. Place UPPER INPUT FREQUENCY (A) selector in the 500 cps - 2.5 kc position.

17. Place PRESET/OPERATE switch in PRESET. Set Frequency/Ratio Counter to read FREQ (A).

18. Adjust VERNIER control for a frequency of 1000 cps. Return PRESET/OPERATE switch to OPERATE.

19. Apply a 100 cps, 2 volt peak-to-peak sine wave to TFM input (J12).

20. Place the OUTPUT FREQUENCY RANGE (B) selector in the 10 - 30 kc range. Set the Frequency/Ratio Counter to read RATIO $\frac{B}{A}$.

21. Turn the OUTPUT FREQUENCY RANGE (B) vernier control fully clockwise, then back counter-clockwise approximately 2 turns.

22. Note the ratio displayed by the Frequency/Ratio Counter. Change TFM input frequency to 1000 cps and again note the ratio displayed by the Frequency/Ratio Counter.

23. Adjust the right hand mica trimmer capacitor so that the ratio remains the same as the TFM input signal is switched between 100 and 1000 cps.

NOTE: The exact ratio reading is unimportant. The point is to obtain a similar reading at both input frequencies.

24. Perform steps 21 and 22 for the remaining output frequency ranges, moving one trimmer capacitor to the left for each successive counter-clockwise output frequency range setting. The adjustments will become less sensitive as the output frequency range switch is moved progressively counter-clockwise.

NOTE: RATIO $\frac{B}{A}$ should be used for the top three output ranges during this alignment phase. Set the counter for RATIO $\frac{A}{B}$ for the four lower ranges.

25. Place TFM/OSC switch in the OSC position. Set the Frequency/Ratio Counter to read FREQ (B). Set OUTPUT FREQ RANGE (B) selector to 30-100 cps.

26. Operate the OUTPUT FREQUENCY RANGE (B) vernier control over its full range, checking to see that signal B adequately covers the 30 - 100 cps range. Adjust the OSC potentiometer (R17) for approximately equal overlap on each end of the range.

27. The unit is now calibrated and ready for use.

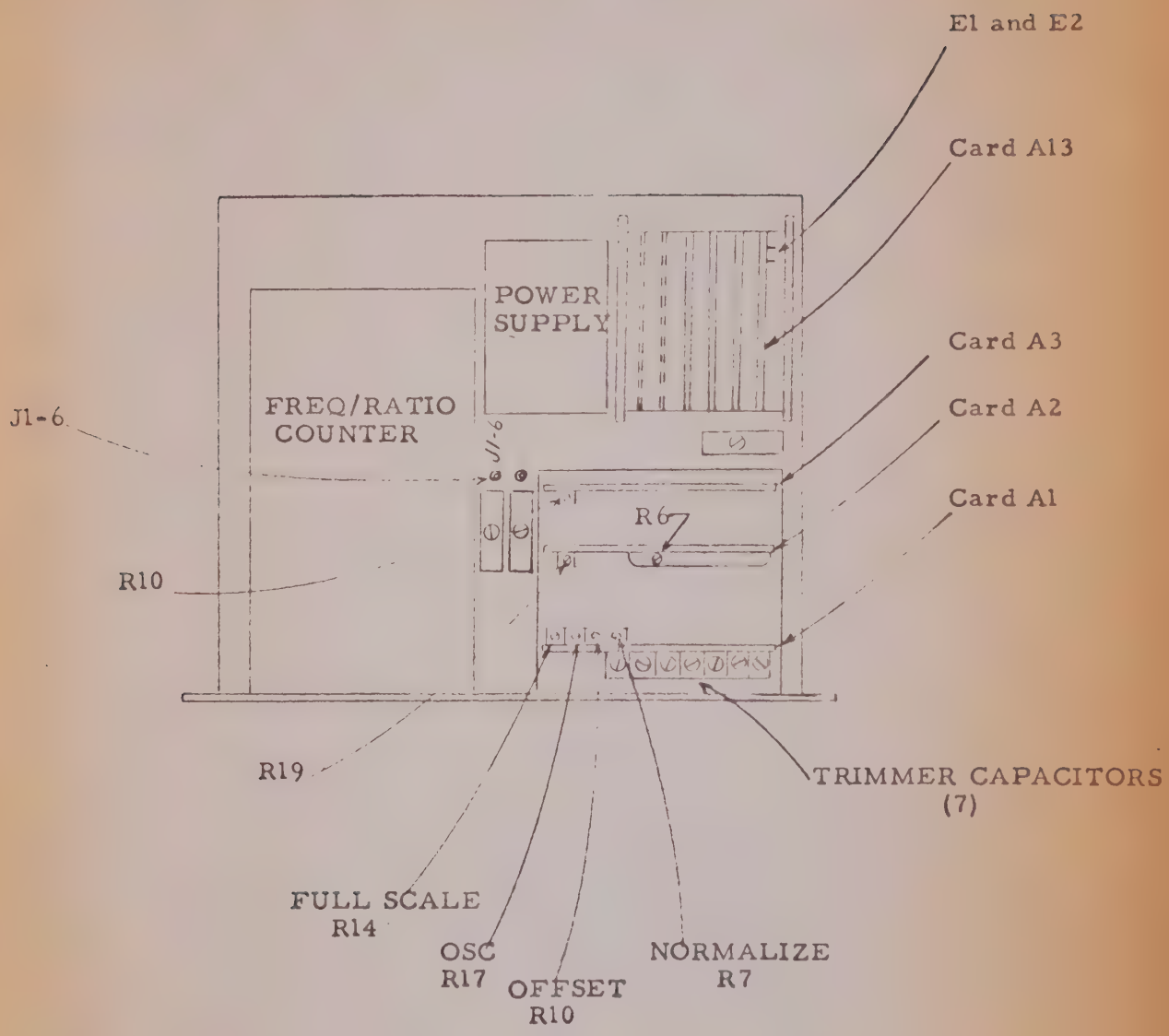
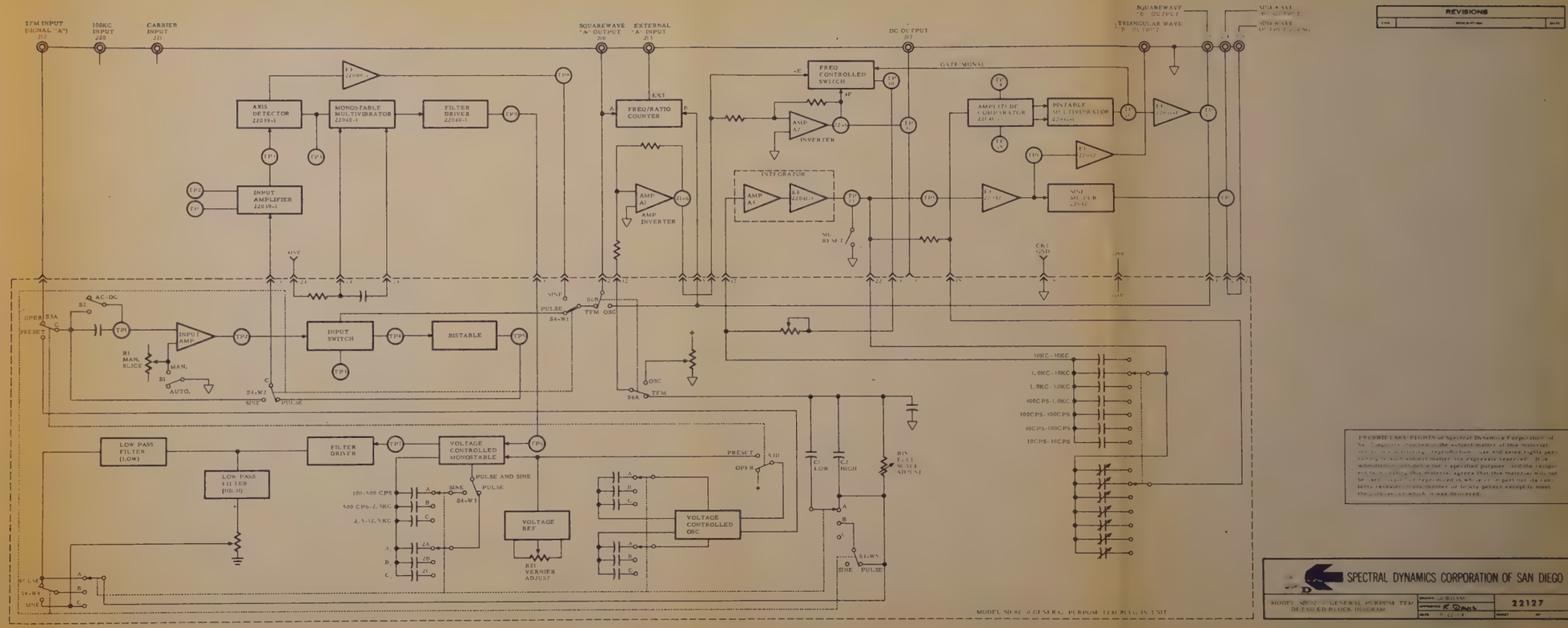


Figure 1. Top View of SD102 and SD102-10 TFM Installed



REVISIONS		
LTR	DESCRIPTION	DATE

PROPRIETARY RIGHTS of Spectral Dynamics Corporation of San Diego, California, in the subject matter of this material (including rights to reproduction, use and sales rights pertaining to such subject matter) are expressly reserved. It is submitted in confidence for operational purposes and the recipient, by accepting this material, agrees that this material will not be used, copied or reproduced in whole or in part nor its contents revealed in any manner or to any person except to meet the limited use for which it was delivered.

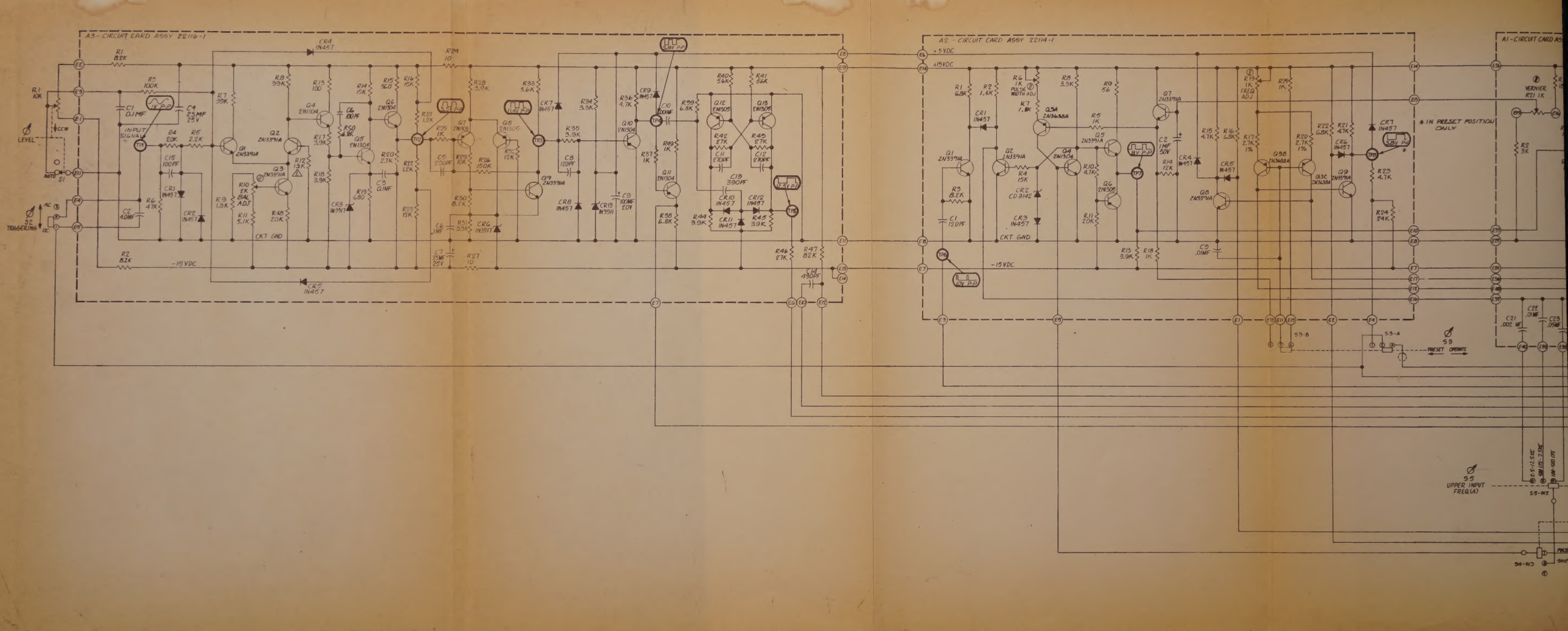
SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

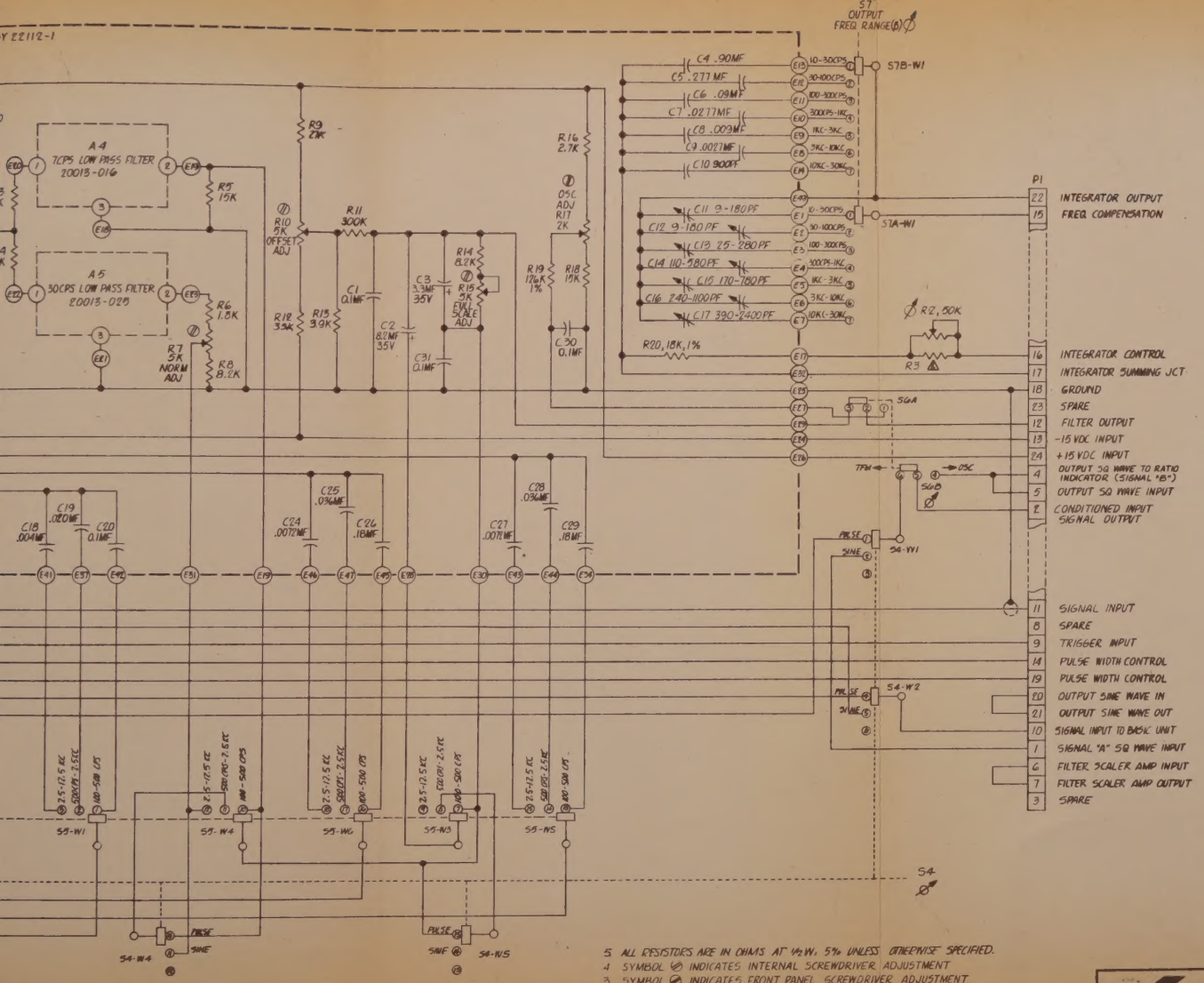
MODEL SD 82 - 3 GENERAL PURPOSE TFM DETAILED BLOCK DIAGRAM

DRAWN: GORDAN
APPROVED: R. Davis
DATE: 6-22-64

22127

SHEET OF


A3 - CIRCUIT CARD ASSY 22116-1
A2 - CIRCUIT CARD ASSY 22114-1
A1 - CIRCUIT CARD ASS
+5 VDC
+15VDC
-15VDC
CKT GND
* IN PRESET POSITION ONLY
PRESET OPERATE
UPPER INPUT FREQ(A)
INPUT SIGNAL
LEVEL
TRIGGERING
VERNIER



REVISIONS		
LTR	DESCRIPTION	DATE
A	PER DRAWN INCORPORATING ALL CHANGES RESULTING FROM ENGINEERING EVALUATION OF SECOND PROTOTYPE. EFFECTIVITY S/N 13 AND UP. S/A	1-20-64 AR
B	CHANGED A1P3 & A1C1 FROM 51K TO 33K. A2C7 FROM 1.7K TO 3.3K. A1C14 FROM 320A TO FACTORY SELECTED 220A. A5P6 FROM 15K SELECTED TO 12K FACTORY ADJUST. A3R1 & A3R2 FROM 12.6K TO FACTORY SELECTED 320. A4R16 FROM 1.5K TO 2.7K PER ECO-162. EFFECTIVITY S/N 15 & UP.	4-6-64 [illegible]
C	CHANGED A2P1 & A2P2 FROM 3.3K TO 1.5K. A2R17 FROM 1.2K TO 2.2K. A1C14 FROM 220A TO SELECTED 320A TO 2.2K/10A. A1C1 FROM 3.3K TO 1.5K. A1P1 & A1P2 FROM 33K TO 27K. A1P4 FROM 68K TO 100K PER ECO-155. EFFECTIVITY S/N 15 & UP.	4-24-64 [illegible]
D	ON CARD AS AND C6 .009MF & RSO G.E.C. ASTRONELL BASE & CORRECTION OF R.S. CHANGE A4R3 FROM 27K TO 33K. CHANGE A1C1 & A5R1 FROM 2.2A FACTORY SELECT TO TYPE 352A PER ECO-158. EFFECT. S/N 17 & UP.	5-1-64 [illegible]
E	ADDED ECO-188. EFFECTIVITY S/N 87 & UP. GARCIA	9/14/64

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

MODEL SD107-10 GENERAL PURPOSE TRACKING FREQUENCY MULTIPLIER

DRAWN A. W. RADDO | 22104 | E

SCALE 1 = 1 | SHEET 1 OF 1